Ultimate
User Manual

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Ultimate chip			
Version	Date	Description	Comments
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1 Suze and main sequencer

1.1 General description of STAR CMOS pixel sensor

Ultimate is the final sensor chip for the upgrade of STAR inner layer of the vertex detector. Its architecture integrates main function of Mimosa26 (Monolithic Active Pixel Sensor (MAPS) with fast binary readout) and including a zero suppression logic. The sensor consists of a matrix composed by 928 (rows) x 960 (columns) pixels of 20.7 µm pitch for a size of the chip of 20.22 mm x 22.71 mm. The design process Austria Micro System AMS-C35B4/OPTO uses 4 metal- and 2 poly- layers. The thickness of the epitaxial layer stretches out up to 15 µm in Hi-Resistivity substrate (400 Ohm.cm).

The design tools follow the CADENCE DFII 5.1 with DIVA, ASSURA, CALIBRE rules. The chip has been submitted in an Engineering Run via CMP on 20 January 2011

In the STAR vertex detector, the hit rate is evaluated at 2.4 x 10^5 hits/s/cm². The design of the sensor is driven by the high readout frequency in order to keep the track multiplicity per frame at a low level. It is done by read out pixel columns in parallel, row by row. The chip readout time is 185.6 µs. Each pixel includes an amplification and Correlated Double Sampling (CDS) and each end of column is equipped with a discriminator. The threshold of the discriminator is programmable by slow control.

After analogue to digital conversion, digital signals pass through the zero suppression block. The digital signals are processed in parallel on 15 banks, then arranged and stored in a memory row by row. Two memories banks have been implemented in the sensor to perform read and write operations simultaneously (see §Memory management).

At each frame, the circuit sends a specific marker to initialize the formatted readout and inside the data, some specifics words give also synchronization markers to begin and start the readout.

The chip offers the choice of the output bit rate of the communication. 160 or 80 Mbits /second.

The configuration by JTAG protocol allows the programming of the test, the masking and the control of the discriminator.

A self in built test is included in the chip for debug of all main digital parts.

(see Figure 1 : Ultimate functional view).

1.2 Architecture description

The core digital includes two main parts called ult_manager and suze.

The first part ult_manager contains:

- the jtag controller treating the configuration registers for the matrix readout (both analog and digital part),
- for testability the command of the possibility to disable the discriminators,
- the pixel sequence read-out block managing the sampling of the pixel,
- the matrix analog readout sequence,
- the mode selection for suze input, the user choices the readout of the analog matrix, the virtual matrix generated by the repetition of 2 lines pattern given, or the synchronization test frame.

The second part suze contains:

- the sparse data scan (sds) extracting by block up to 6 hits (for the line up to 6 x15),
- the second stage the mux6x15 to 9 retains 9 states from the previous one,

- the main sequencer a key component of the chip generates all the synchronization signals for the line the operations inside the line and for the whole frame. It produces also the line address counter. In running mode, it reaches maximum 928 lines.
- the boundary scan chain for testing the main input and output pads,
- the memory management sequencing the writing and reading operation,
- the ram (4 memories of 2048 x 16 bits)
- additional test structure acting as a probe for each block,

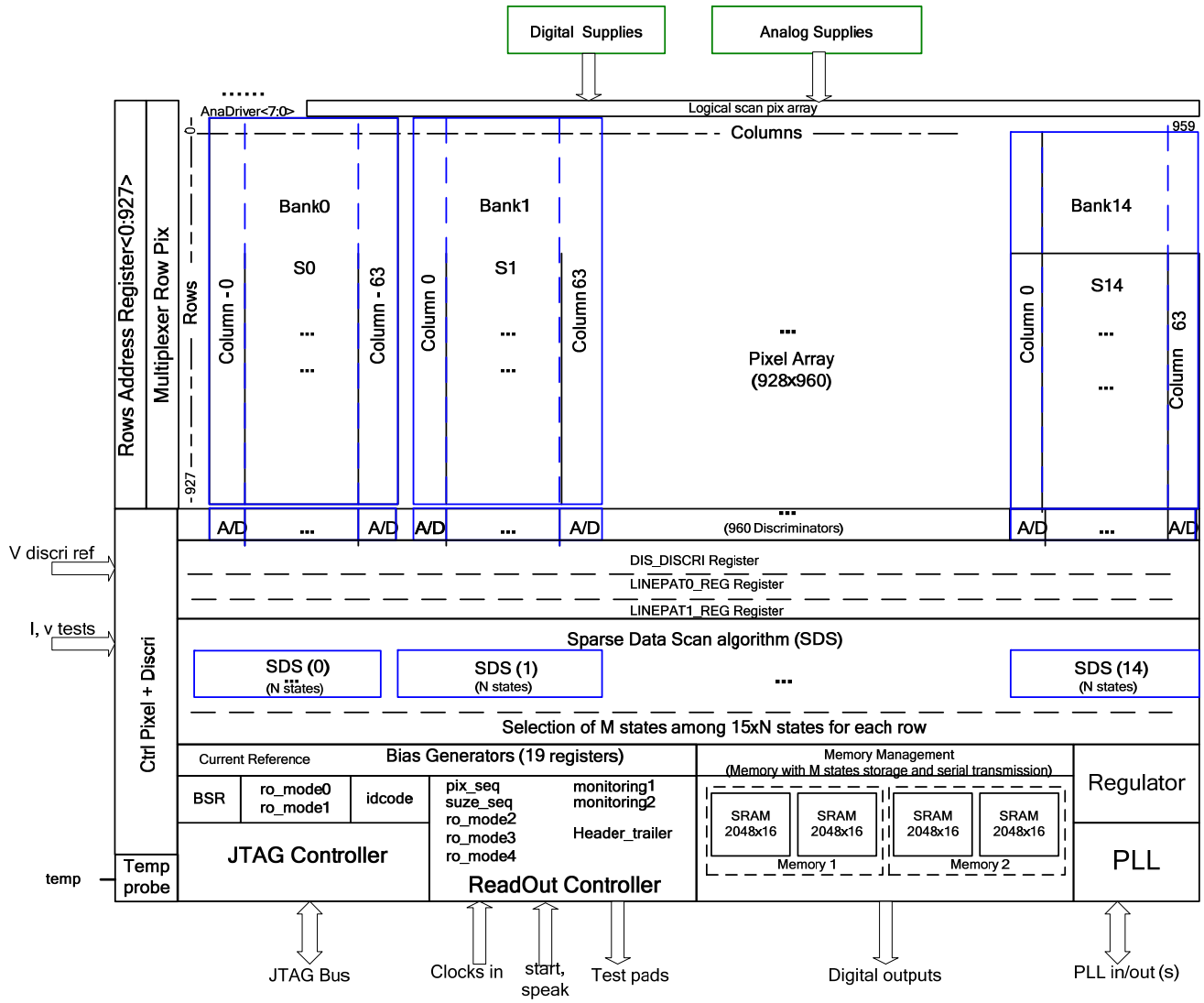


Figure 1 : Ultimate functional view

1.3 Ultimate main synoptic

The following synoptic shows the implementation of SUZE into Ultimate.

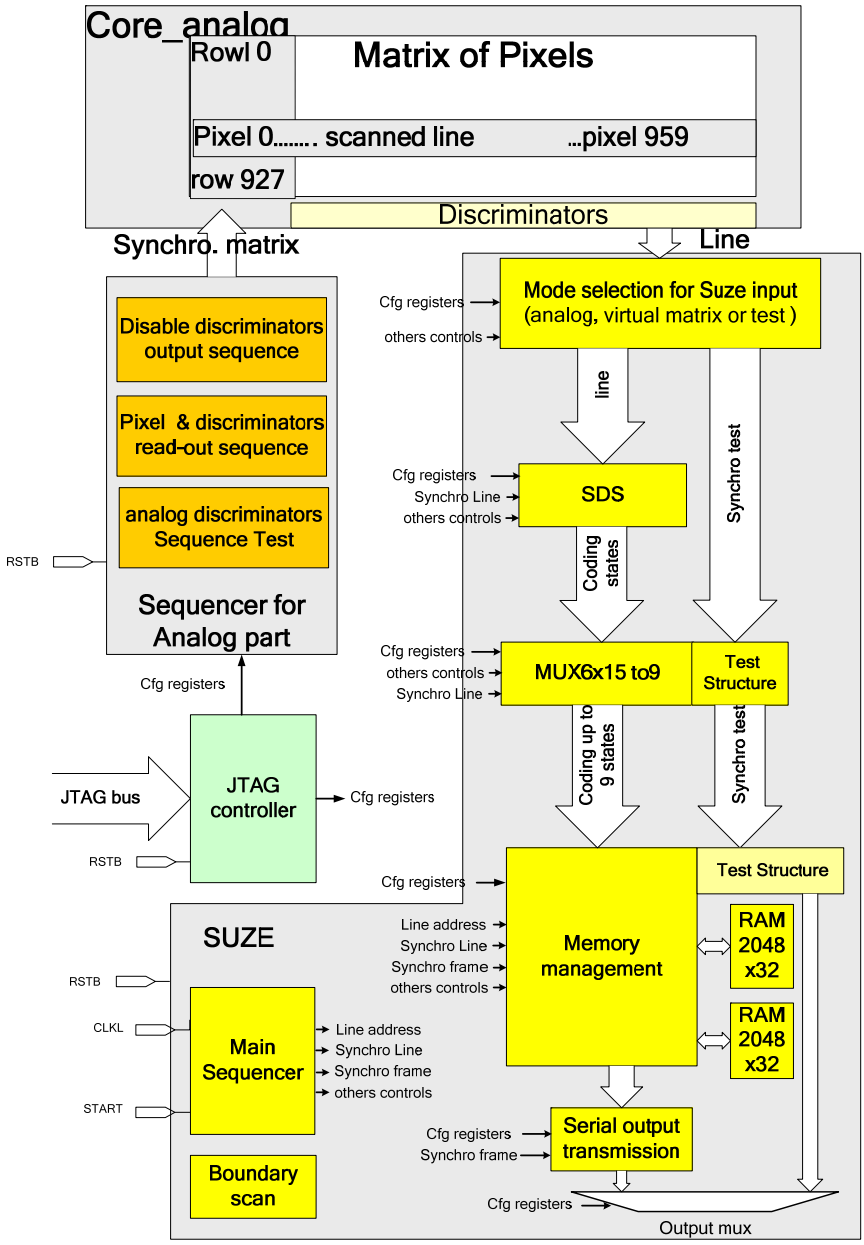


Figure 2: top view implementation of SUZE in ULTIMATE

This digital part manages sequentially each line for the whole frame composed of 928 lines x 960 columns. The main sequencer gives to the structure the address of lines and all synchronizations and controls signals.

A JTAG controller brings the configuration information. (Table of configurations registers) A test structure simulates a matrix of pixel in order to check the functions of SUZE.

1.4 Synoptic of SUZE

This digital part includes 3 main parts:

- The Sparse Data Scan (SDS),
- The multiplexer,
- And the memory management.

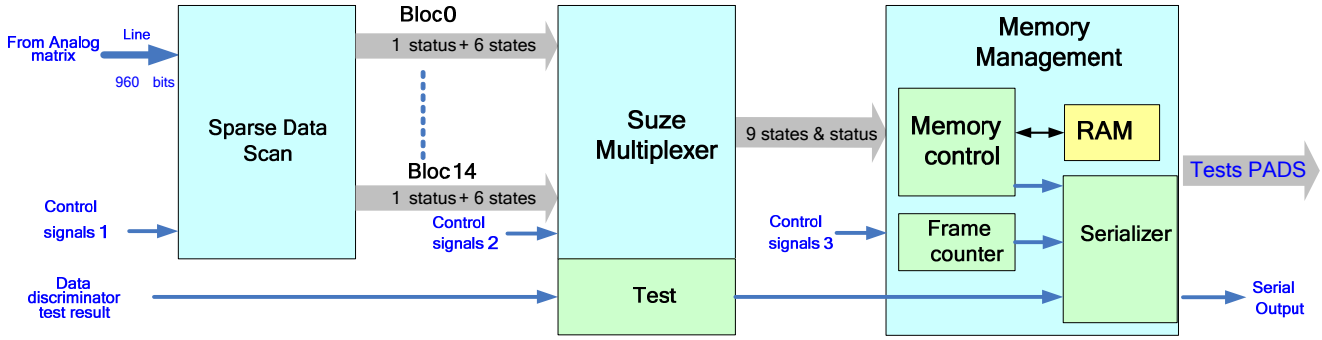


Figure 3: SUZE block diagram

1.5 SPARSE DATA SCAN (SDS)

1.5.1 Introduction

Based on a sparse data scan algorithm to find hit pixels (discriminator output = "1"), this module Sparse Data Scan (SDS) receives a line constituted of 960 pixels (959 to 0) divided in 15 blocks of 64 pixels.
Up to 4 contiguous pixel signals above $V_{threshold}$ of the discriminator will be encoded in a 2 bits state word following the address of the 1st pixel

Block	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pixels per block	959 – 896	895 -832	831 – 768	767 – 704	703 – 640	639 – 960	575 – 512	511 – 448	447 – 384	383 – 320	319 -256	255 -192	191 -128	127- 64	63-0

Each block extracts of the 64 pixels bus:

- 1 status group,
- 6 states, (column addresses + encoded state)
- 1 overlapping.

These 15 blocks works in parallel and give 6 x 15 states to the next stage.

1.5.2 One block description

The next figure shows the different steps of the sparse data scan for one block.

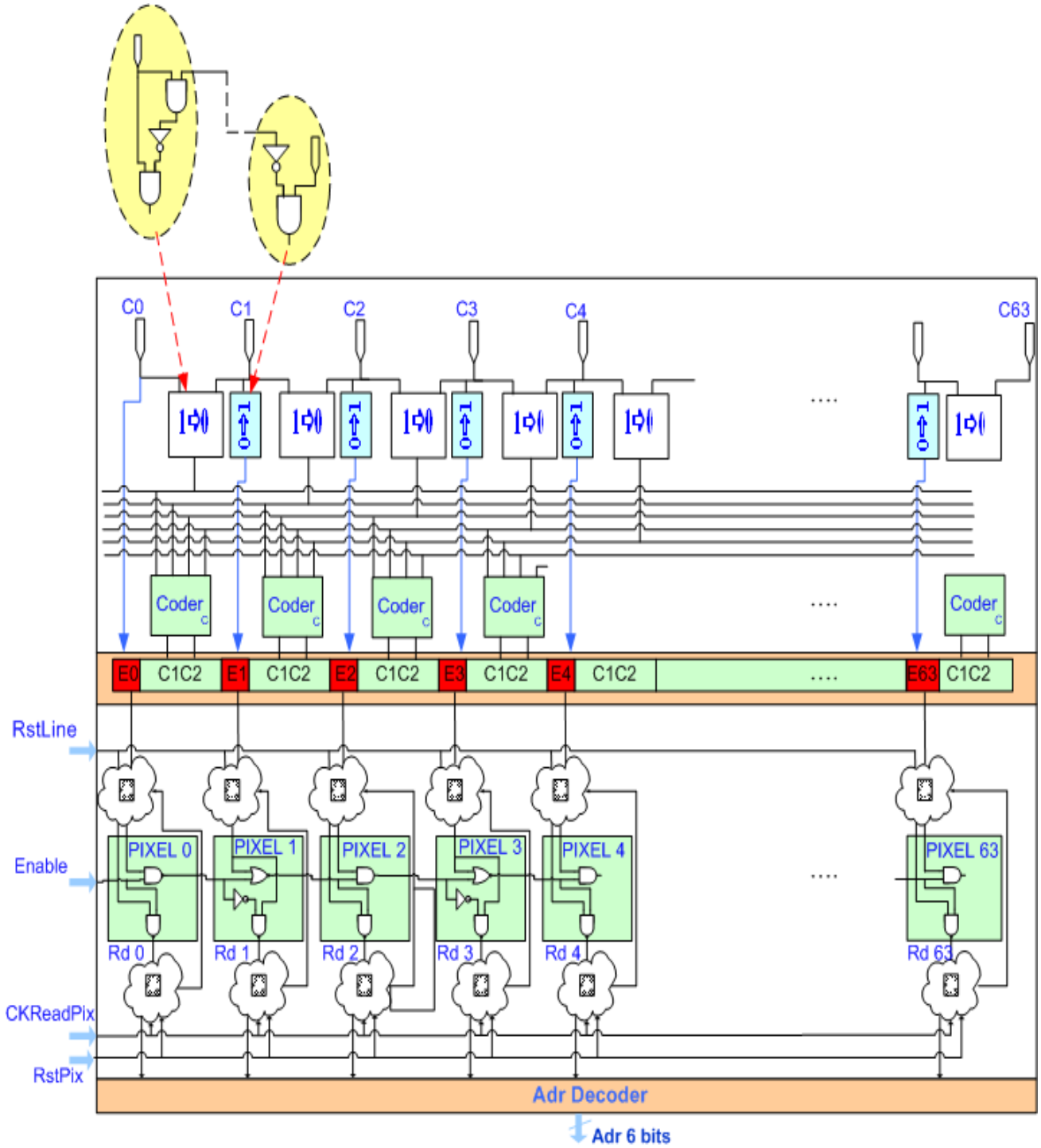


Figure 1: Schematic view of sparse data scan for one block

The algorithm proceeds through four consecutive steps, summarized below:

- In the first step, the data inputs for the process are extracted from 64 discriminators;
- The second step consists in encoding groups of hit pixels.

This logic provides Enable bits and Code bits for each column composing a bank. The Enable bit is set to 1 for the first hit pixel in a group. The number of Enable bits set to 1 characterizes the state;

- The third step selects the “states”; each “state” is selected successively by a sparse data scan. It uses a chain of alternated NAND and NOR gates for the priority management during the sparse-scan. The generation of “states” requires several instructions. The number of “states” (N) in a bank is related to M “states” in a row. The algorithm manages up to N = 6 instructions or “states” in a bank;
- At each instruction, the column address of the “state” is decoded. The last digital step stores the N “states” and generates “status” information indicating the number of “states” per bank. Each bank has its own address encoded in 5 bits.

1.5.3 Timing diagram for control signals

These inputs signal are given by the main sequencer

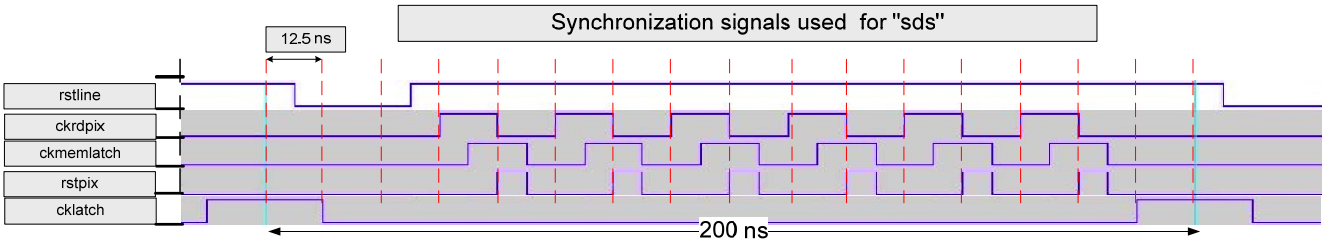
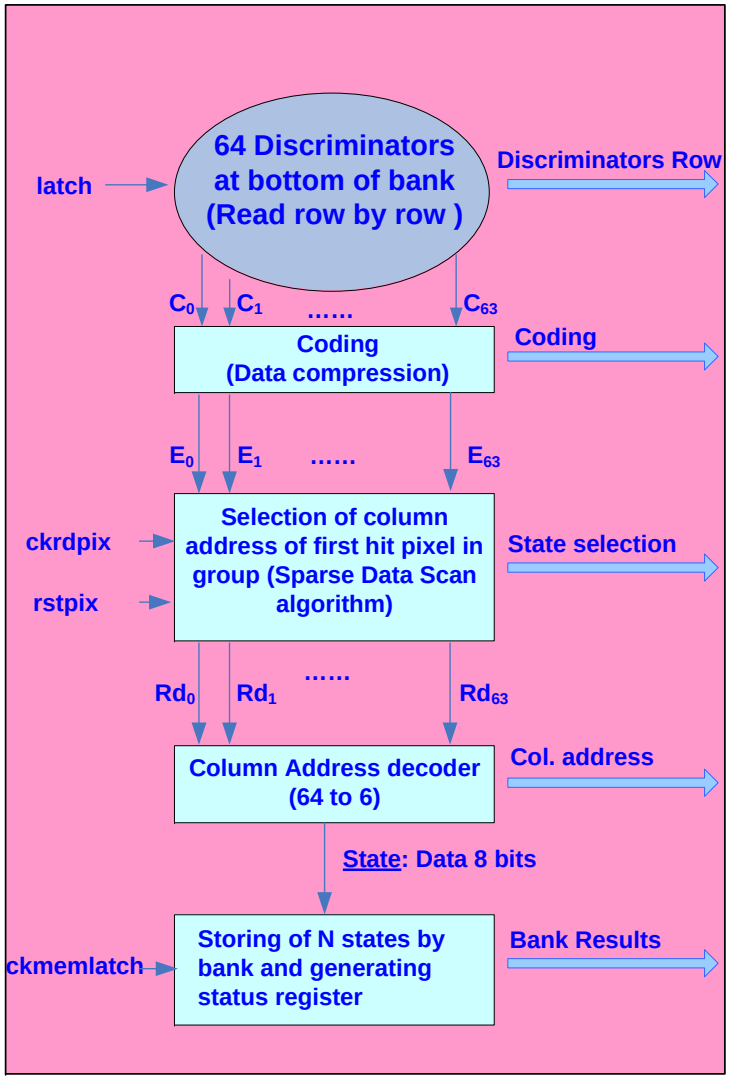
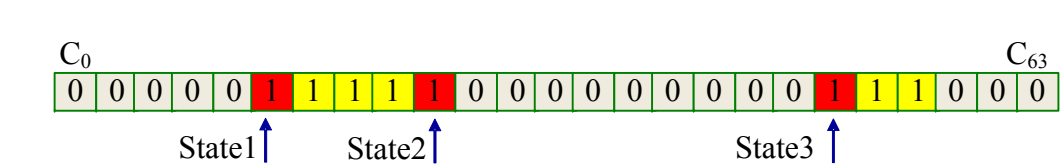


Figure 4: Synchronization signals for SDS timing diagram

1.5.4 Algorithm sparse data scan (SDS) description

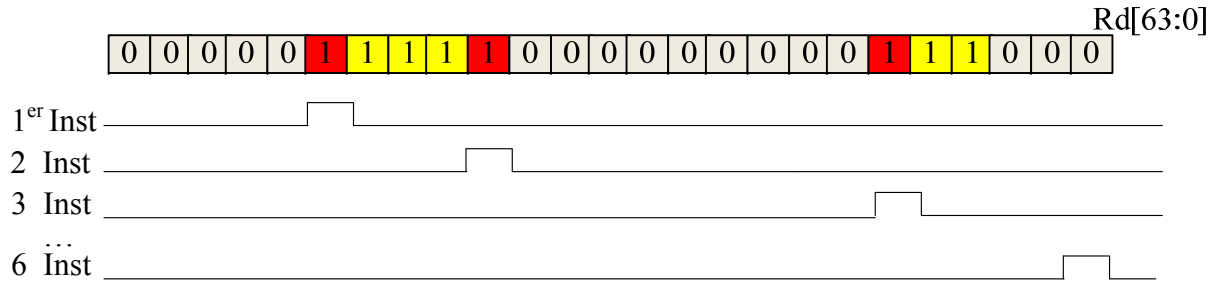




By Column: ① Enable : 1 bit

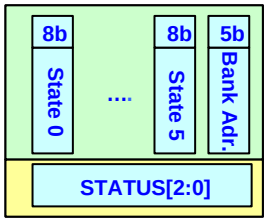
Enable bit is set to 1 for first hit

② Code: 2 bits Pixel in group



This is the sequence used to decode column address of first hit pixel in group, it's corresponding to read enable bit which is set to '1'. The number of instruction is limited at 6

Each state is composed of 6 bits Column address plus 2 bits code



- Maximum 6 States registers of 8 bits
- Bank address register of 5 bits
- Status register of 3 bits (number of states by bank)

1.5.5 Synoptic

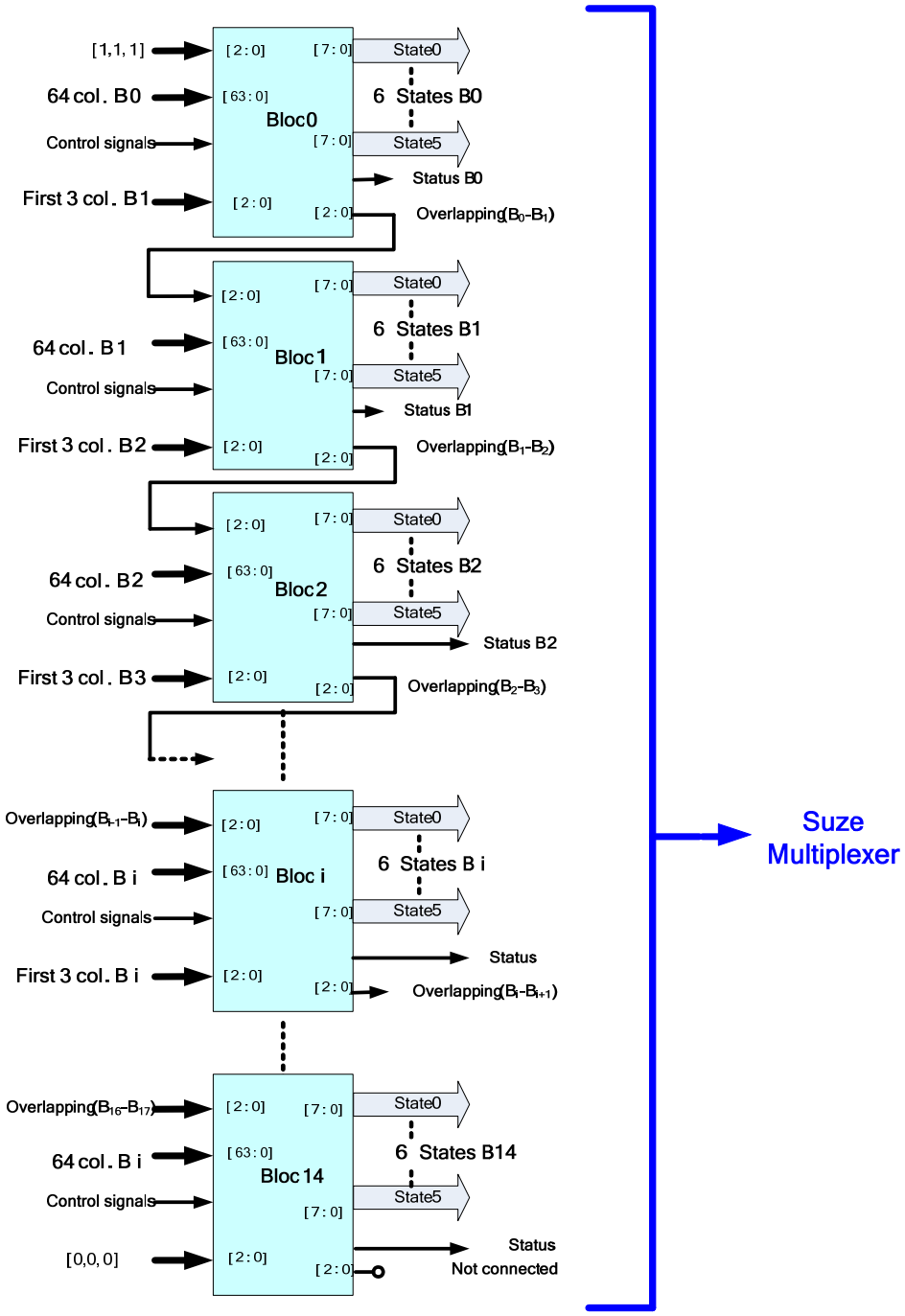


Figure 5: SDS block diagram

1.5.6 Coding

The following table shows the format of the result for one block.

	State 0									State 1								State 2							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
0	1	2	0	1	0	1	2	3	4	5	0	1	0	1	2	3	4	5	0	1	0	1	2	3	4	5
Status block			coding		Column address						coding		Column address						coding		Column address					

State 3								State 4								State 5								new_bit210j		
27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53
0	1	0	1	2	3	4	5	0	1	0	1	2	3	4	5	0	1	0	1	2	3	4	5	0	1	2
coding			Column address					coding			Column address					coding			Column address					Overlapping		

Figure 6: format of the SDS results

For the whole line, we have 15 x (1 status blocks and 6 states).

1.6 States multiplexer

1.6.1 Introduction

The states multiplexer reads out the outcomes of the 15 banks x 6 states and keep up maximum 9 states from the previous stage SDS.
Three objects constitute this block:

- 2 identical modules (Mux 6x8 ➔9) which extract each one 9 states and 1 status for an half line
- 1 module (Mux 2 x 9 ➔ 9) which retains 9 states and a status from these 2 modules

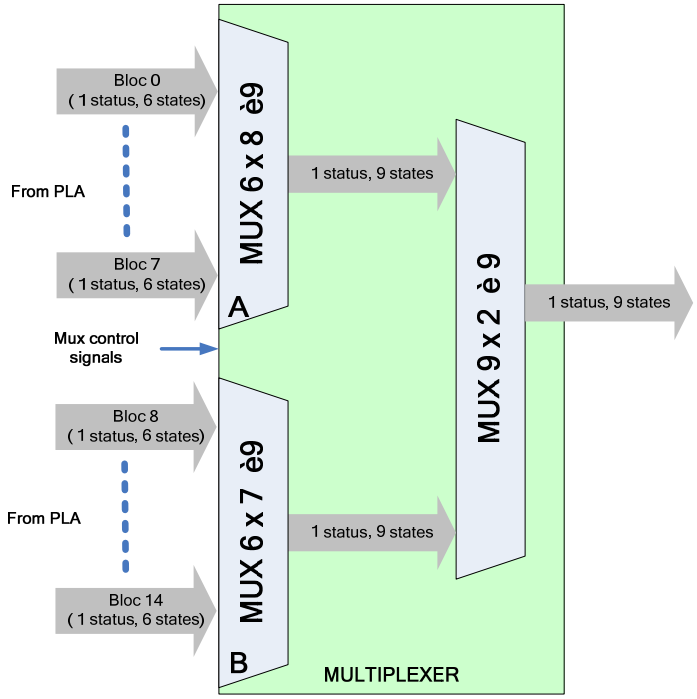


Figure 7: Multiplexor top view

Sample signals
This synchronous module uses 3 signals

- The first one initiate the process: rstline
- The second one samples the selection of the hit kept: ckrdpix
- The third one en_fsm_mux signal latches the record states.

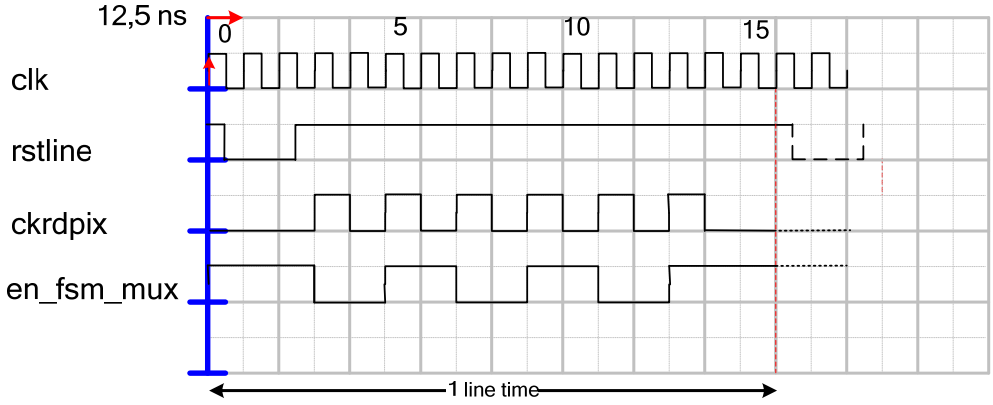


Figure 8: Synchronization signals for MUX 6 x 8 ➔ 9 , MUX 6 x 7 ➔ 9top view

Figure 9: Module 6 x 9 ➔ 9 top view

1.6.2 Coding

The following table shows the format of the result for the line given to the memory management.

State 0													State 1													
3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
3	0	1	2	3	4	5	6	7	8	9		15	0	1	0	1	2	3	4	5	6	7	8	9				
	Row											OVF	Coding						Column									

State 2													State 3													
35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	2	3	4	5	6	7	8	9					0	1	0	1	2	3	4	5	6	7	8	9				
	Column												Coding						Column									

State 4													State 5													
67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	2	3	4	5	6	7	8	9					0	1	0	1	2	3	4	5	6	7	8	9				
	Column												Coding						Column									

State 6													State 7													
99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	2	3	4	5	6	7	8	9					0	1	0	1	2	3	4	5	6	7	8	9				
	Column												Coding						Column									

State 8													State 9													
131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	2	3	4	5	6	7	8	9					0	1	0	1	2	3	4	5	6	7	8	9				
	Column												Coding						Column									

Figure 10: format of the multiplexer results

1.6.3 Module 6 x 8 ➔ 9 and module 6 x 7 ➔ 9

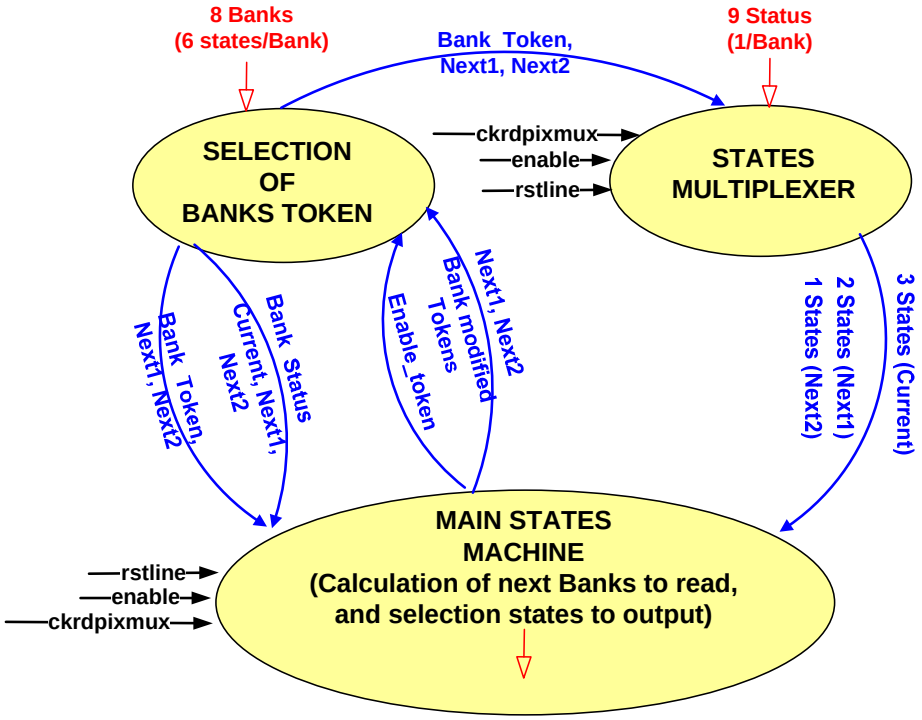


Figure 11: Module 6 x 8 (or 6 x 7) ➔ 9 top view

Construction of the address column of the hit state:

Each block of 64 pixels gives an address on 6 bits (0:5) added with the address of a group on 4 bits (0:3). The total of the line address includes 10 bits (0:9).

Given the critical timing constraints, we subdivide the line (960pixels) in 2 block of (8 banks x 64 pixels) working in parallel with the same constraints in the layout.(1 bank is inactive).
To respect this symmetry, little craftiness consists of adding the value 512 (8 x 64) to the column address for each state inside the module states multiplexer 6x8 ➔9.

Systematically, the next module (mux 9 x 2 to➔ 9)will correct the address column of each calculated state coming from the first bank Mux 6x8 ➔9 by the removal of 512.

$$\textbf{Column address} = \textbf{pixel address into the block} + \textbf{address of the block}$$

Calculation of the number of states hit per half line
A function totals up all the number of state per bank given by the previous stage SDS.
If the total exceeds 9, the result will keep this value and the overflow flag will print 1.The equation below resumes the calculation.

$$Nb\_states/line = \sum_{i=0}^{8} Nb\_states_{Bank_i} \leq 9$$

Selection of the 9 states inside the module Mux 6x8 ➔9
First between each rising edge of ckrdpix signal, three successive token identifies each one asynchronously the position of the next hit state according to a pyramidal structure from the left significant position of the pixel (position 0 of the column) to the most significant position (position 512).

Token 1: it points at the first state hit not taken in account before whatever the location inner and inter bank
(from column 0 to 959).

Token 2: it locates the fourth hit state following the token 1 if this state is included into the same bank of the cursor 1.
The third or second hit state if the state belongs to another bank of the token 1.
On the last hit state if no hit happens.

Token 3: it points at the third hit state following the token 2 if this hit state belongs to the same bank as token 2.
On the last hit state if no hit exists anymore.

This process allows the management and recording of three ready states for the next rising edge of the signal enable_mux done on next module.

The picture below illustrates the token's processing according to the synchronization signals.

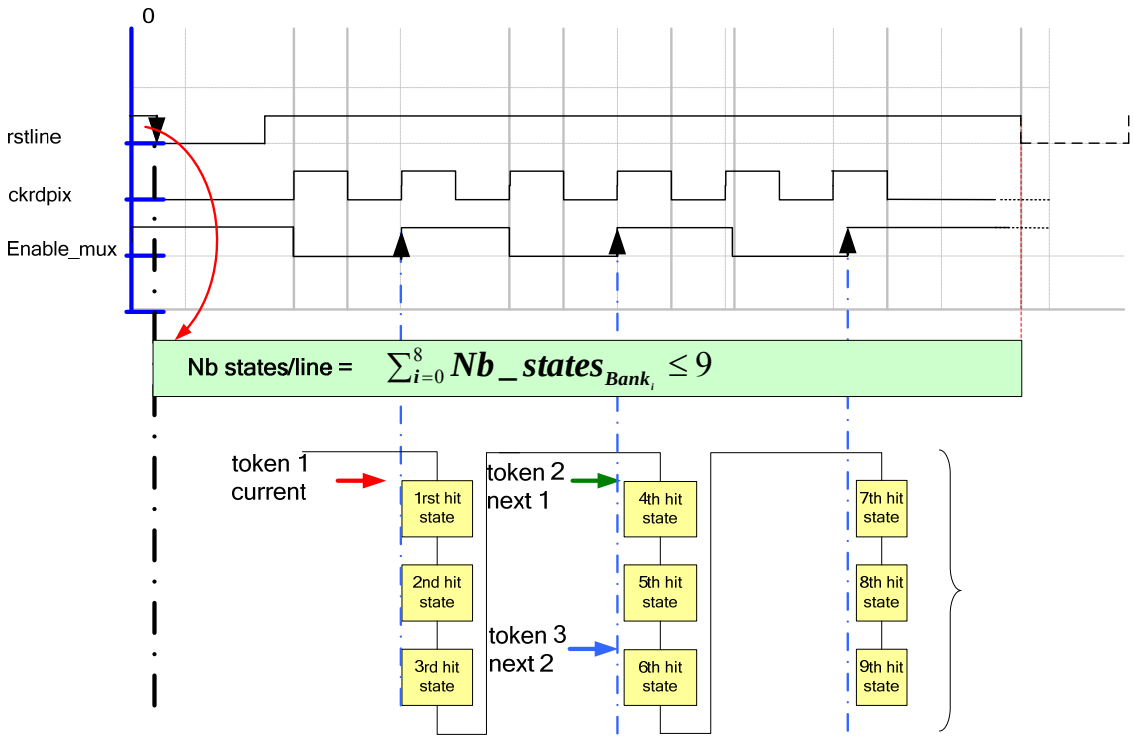


Figure 12: token's processing according to the synchronization signal

1.6.4 Module 2 x 9 ➔ 9

This component collects the first 9 states from the two module Mux 6x8➔9

A state machine (fsm) initiated by the synchronization line event signal (rstline low level active), records the 9 states in 3 times latched by the signal enable_mux (3 states each rising edge of enable_mux signal).

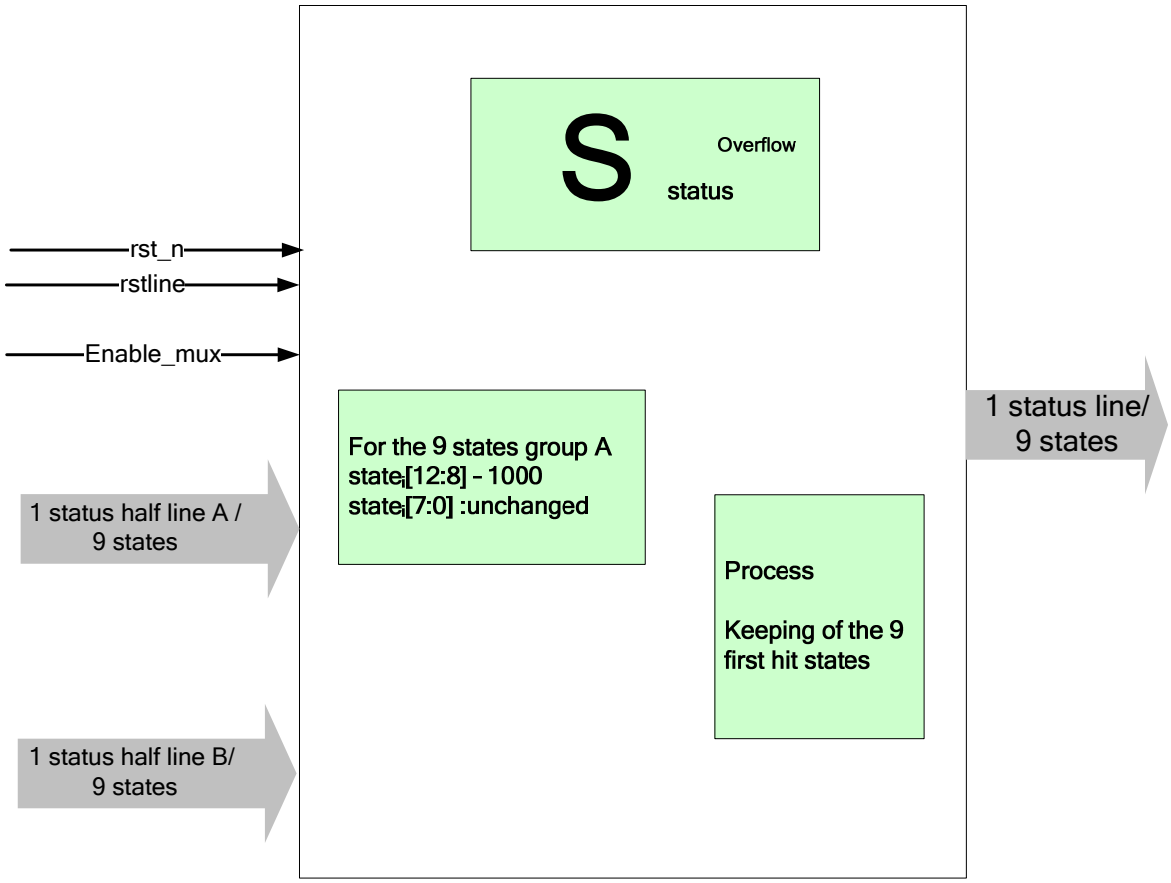


Figure 13: Module 6 x 9 ➔ 9 top view

1.7 Memory management

1.7.1 Memory control + multiplexer test + RAM

1.7.1.1 Introduction

This stage bufferizes the data coming from the previous stage before their transmission to outside.
The management of the memory is a classic one, using single access RAM.
The writing and reading are totally separated. The minimum writing cycle time is 25 ns and the reading 100 ns. The worst specification of these RAM (IP AMS) is 5 ns for both read/write mode cycle.
The paths with the worst constraints (75°C, 3V & 2.7V) are controlled.

The relative complexity of the writing mode is dictated by the optimization of the memory depth and the stored data flow, variable according to the number of hits by row.

No possible crash of the reading by the writing operation. Only one frame top start information toggles the writing from the reading mode.

The pipeline of the writing mode minimizes the consumption as lower as possible.(160 bits in 200 ns)

The writing time of the whole matrix is extended at maximum, i.e. a frame time operation (185 µs) minimizing the delay constraints (technology and layout) and the consumption.

Only the final block (shift registers: less than 50 flipflops) is sampled with 160 MHz frequency.

1.7.1.2 Top view diagram

The top view diagram or synoptic represents how the architecture is structured around the memory.
A latch receives the data from the multiplexer stage (9 states, 1 status line).
The memory writing module manages the writing into the memory according to the contents of the data.
A special sequence is done to optimize the space into the memory, critical part of this design for the implementation (timing constraints)

.

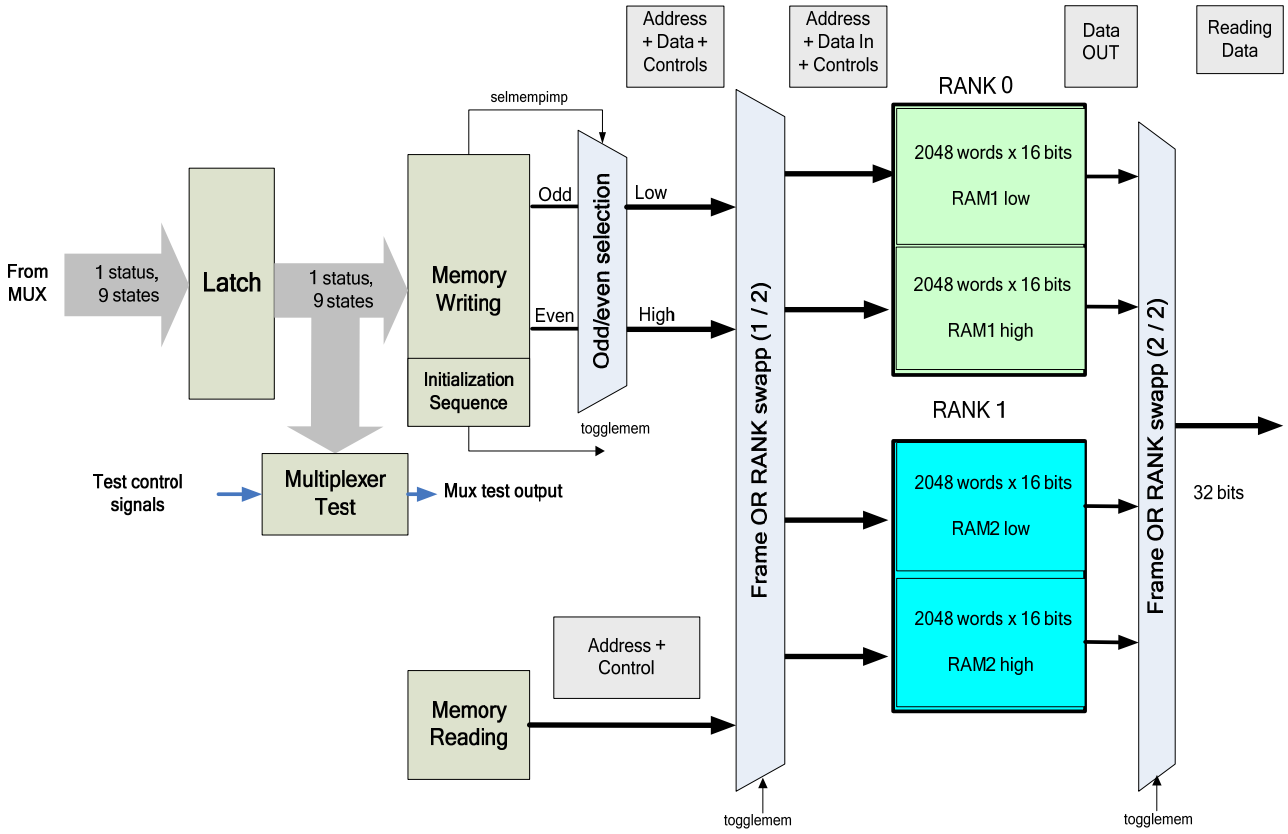


Figure 14: Memory management top view

NB: The multiplexer test explained later in the test part uses the first stage of the memory manager.

1.7.1.3 Working mode

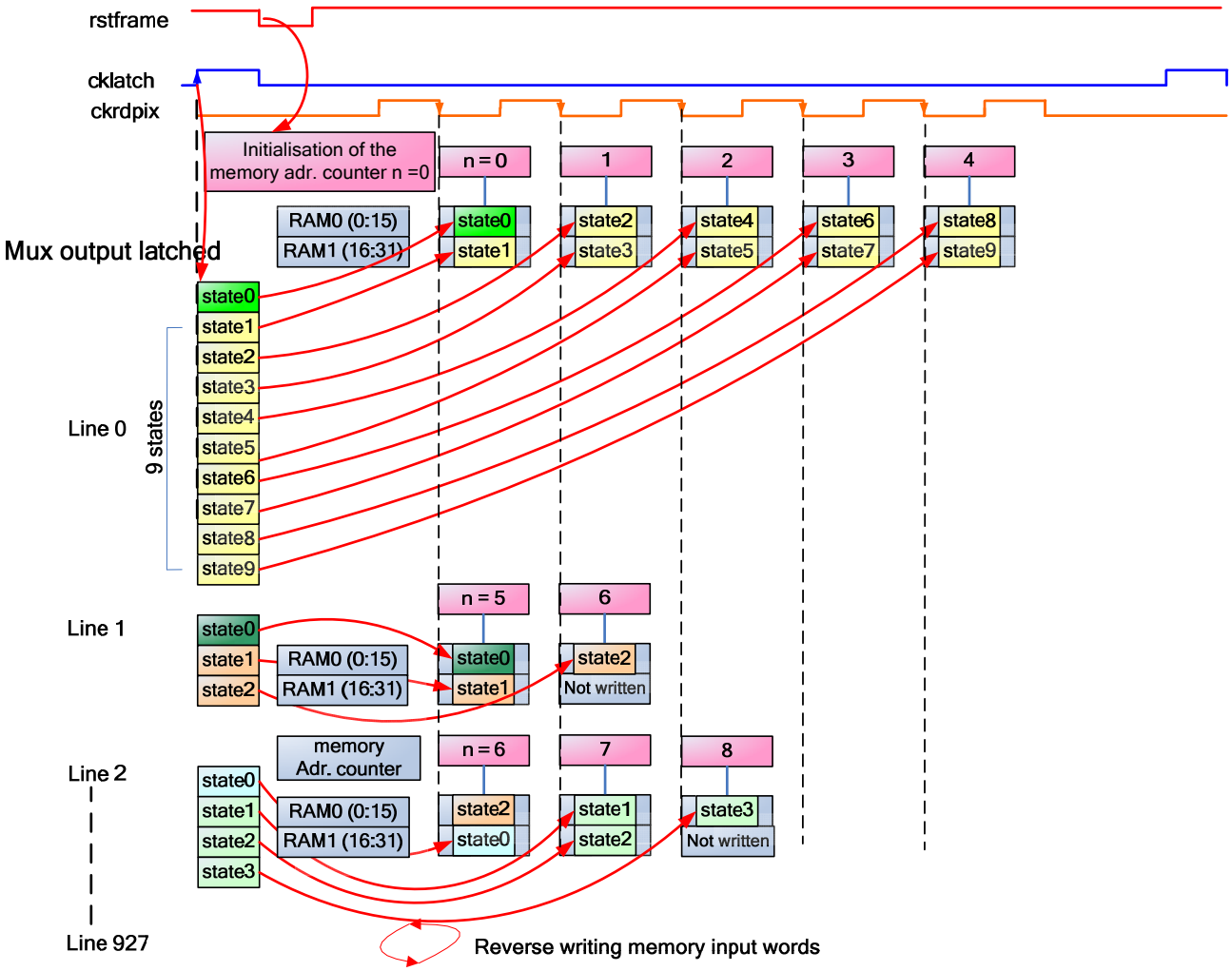


Figure 15: Odd/even swapping working mode procedure

The memory space includes four single access RAM 2048 words of 16 bits (IP from AMS) to ensure the continuous read-out. The writing and reading mode represent two independent blocks.
The process fills up the memory only when the data appears.
The memory stops to fill up when no new hit is detected, the memory is full or at the end of the frame.
According to the data received, the completion rate of the memory can change from a frame to another one.

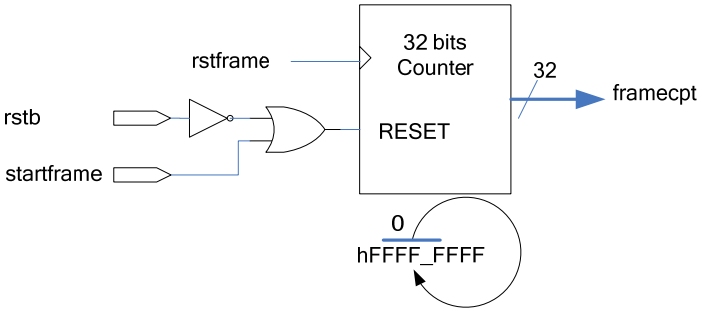
- During the current frame, the writing mode uses 2 SRAM's while the reading mode works with 2 others SRAM's.
- The writing process is realized by the writing of word of 2x16 bits. In order to reduce the useful memory space (see Figure 13), if the last word of 16 bits is not written (in case of even number of hit states in the current row), next row processing status is written in that location.
- At the end of the frame, a state machine memorizes the number of written words given by the address writing counter.

During the next frame, the 2 operations (reading/ writing) are swapped, and this process is repeated at each frame.

The format of the row “states” is composed of Status/line and State words. *States/Line* contains the address of the hit line, the number of “state” for this line (i.e. a number between one and nine), and an overflow flag. “State” contains the address of the first hit pixel and the number of successive hit pixels.

1.7.2 Frame counter

This frame counter initialized at the reset works from 0 to FFFF_FFFF and restarts from 0.
Each occurrence of the falling edge of rstframe increments the counter.



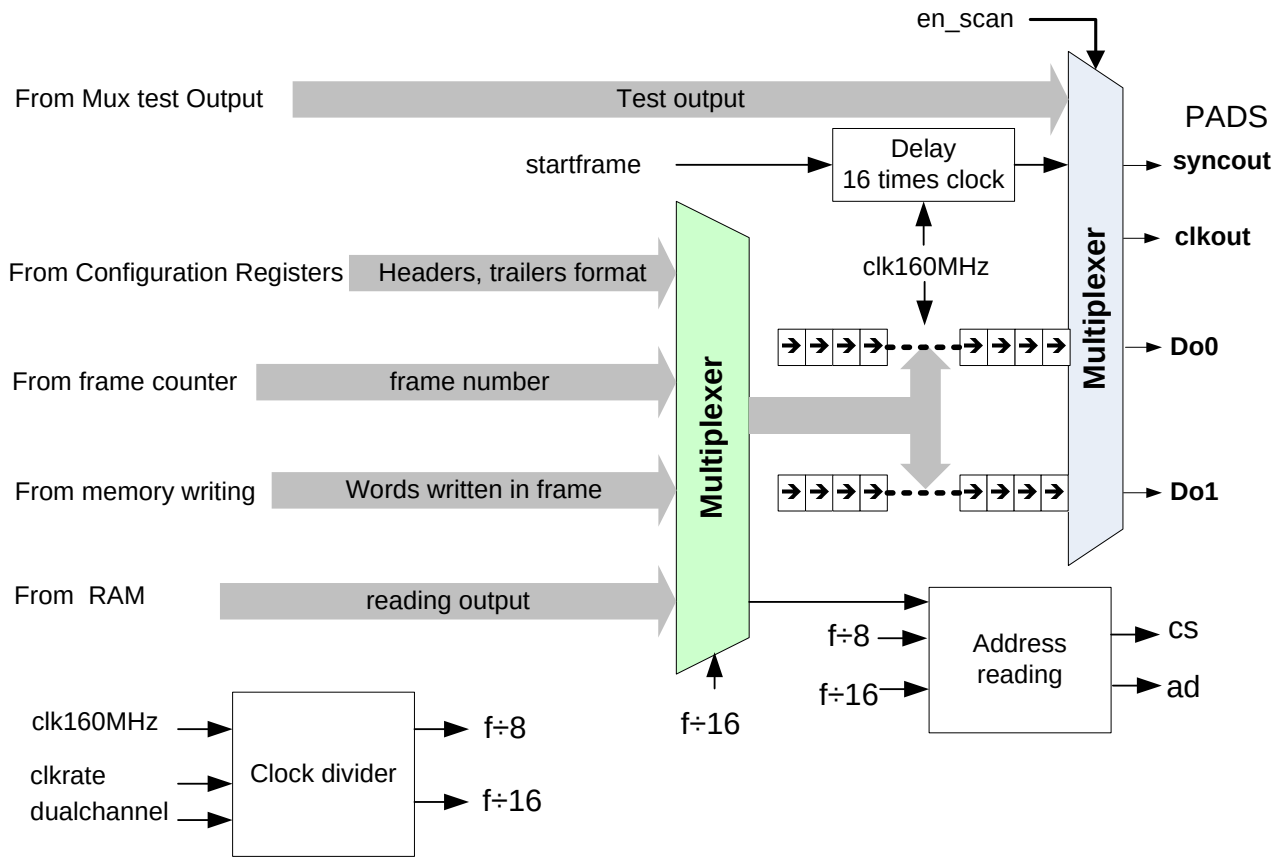
The re-initialization of the counter is done by setting the register en_startframe to 1 and to 0 (ro_mode1 register).

1.7.3 Serializer and data format

This stage formats the data to the output ports, and selects the normal working or test mode.

If en_scan:

- = 0 please refer to the normal mode data format paragraph 3.5.1
- = 1, please refer to the test mode paragraph 3.5.3,



2 Control Interface

2.1 Introduction

The JTAG controller works independently of the main external clock and asynchronously.
AT the end of the JTAG communication, the user can access to the initialization of the sequencer by the start sequence.

The control interface of Ultimate complies with Boundary Scan, JTAG, IEEE 1149.1 Rev1999 standard. It allows the access to the internal registers of the chip like the bias Register and the different registers control.

2.2 JTAG Instruction Set

After the main reset sequence, the user must load into the Instruction Register of the JTAG controller the code of the desired operation to perform or with the code of the desired data register to access.

Instruction	5 Bit Code$_{16}$	Selected Register	Notes
extest	01	bsr	JTAG mandatory instruction
highz	02	bypass	JTAG mandatory instruction
intest	03	bsr	JTAG mandatory instruction
clamp	04	Bypass	JTAG mandatory instruction
sample_preload	05	bsr	JTAG mandatory instruction
id_code	0E	dev_id	User instruction
bias_gen	0F	the bias_gen	datareg0
patt_line0	10	Pattern_line0	datareg1
dis_disc	11	Disable discriminator line	datareg2
pix_seq	12	seq_pix	datareg3
monitoring1	13	monitoring1	datareg4
patt_line1	14	Pattern_line1	datareg5
suze_seq	15	sequencer_suze	datareg6
header_trailer	16	Headers	datareg7
Monitoring2	17	ctrl_suze	datareg8
NU1	18		datareg9
NU2	19		datareg10
ro_mode4	1A	Read out mode 4	datareg11
ro_mode3	1B	Read out mode 3	datareg12
ro_mode2	1C	Read out mode 2	datareg13
ro_mode1	1D	Read out mode 1	datareg14
ro_mode0	1E	Read out mode 0	datareg15
bypass	1F	BYPASS	JTAG mandatory instruction

(1) Instruction codes implemented but not the corresponding registers. To be fixed in the next version.

2.3 JTAG Register Set

JTAG registers are implemented with a Capture/Shift register and an Update register.
JTAG standard imposes that the last significant bit of a register is downloaded/shifted first.

Register Name	Size (bits)	Access	Notes
INSTRUCTION REG	5	R/W	Instruction Register
id_code	32	R Only	
Bsr	11	R/W	Boundary scan register
bias_gen	148	R/W	Previous value shifted out during write
patt_line0	960	R/W	Previous value shifted out during write
dis_disc	960	R/W	Previous value shifted out during write
pix_seq	112	R/W	Previous value shifted out during write
monitoring1	30	R/W	Previous value shifted out during write
patt_line1	960	R/W	Previous value shifted out during write
seq_suze	160	R/W	Previous value shifted out during write
header_trailer	64	R/W	Previous value shifted out during write
monitoring2	8	R/W	Previous value shifted out during write
NU1…..NU2	0		Not implemented. For future use
ro_mode4	8	R/W	Previous value shifted out during write
ro_mode3	8	R/W	Previous value shifted out during write
ro_mode2	8	R/W	Previous value shifted out during write
ro_mode1	8	R/W	Previous value shifted out during write
ro_mode0	8	R/W	Previous value shifted out during write
BYPASS	1	R Only	

2.4 Instruction Register

The test Access Port Controller defined by the IEEE 1149.1 standard includes the instruction register (5 bits long).
On reset, it is set with the ID_CODE instruction. During its reading, the 2 last significant bits are set with the markers specified by the standard; the remaining bits contain the current instruction.

X	**X**	**X**	**1**	**0**

2.4.1 DEV_ID Register

The Device Identification register (32 bits long) allows the reading of the fixed hardware value into the chip.
The selection of the ID_CODE instruction causes the shifting of this fixed value to TDO, the JTAG serial output of the chip.Ultimate ID_CODE register value for ULTIMATE is : UT1*1*. 0x55543101

Bit	**Register name**	**Purpose**	**Default value Code$_{16}$**		
31-0	ID_CODE	Device Identification register	55543101	*ASCII*	*HEXA*
				'U'	"55"
				'T'	"54"
				'1'	"31"
				<SOH>	"01"

2.4.2 Boundary Scan Register (BSR)

The Boundary Scan Register, according to the JTAG instructions, tests and set the IO pads.
The Ultimate BSR (11 bits long) allows the test of the following input and outputs pads.

Bit	**Corresponding Pad**	**Type**	**Signal**	**Notes**
10	ext_disc_line	Input	ext_disc_line	Hit emulation (during one line minimum or x lines)
9	ext_pwr_pulse	Input	ext_pwr_pulse	
8	clkc	Input	clk_lvds	CMOS Clock
7	start	Input	start	Readout : Input synchronization
6	speak	Input	speak	Initial control for JTAG communication
5	clka_mk	Input	clka_mk	Clock marker for analog part
4	clka	Input	Clka	Clock for analog part
3	pad_syncout	Output	Syncout	Synchronization output
2	pad_clkout	Output	Clkout	Clock output
1	pad_do0	Output	pad_do0	Data output pad 0
0	pad_do1	Output	pad_do1	Data output pad 1

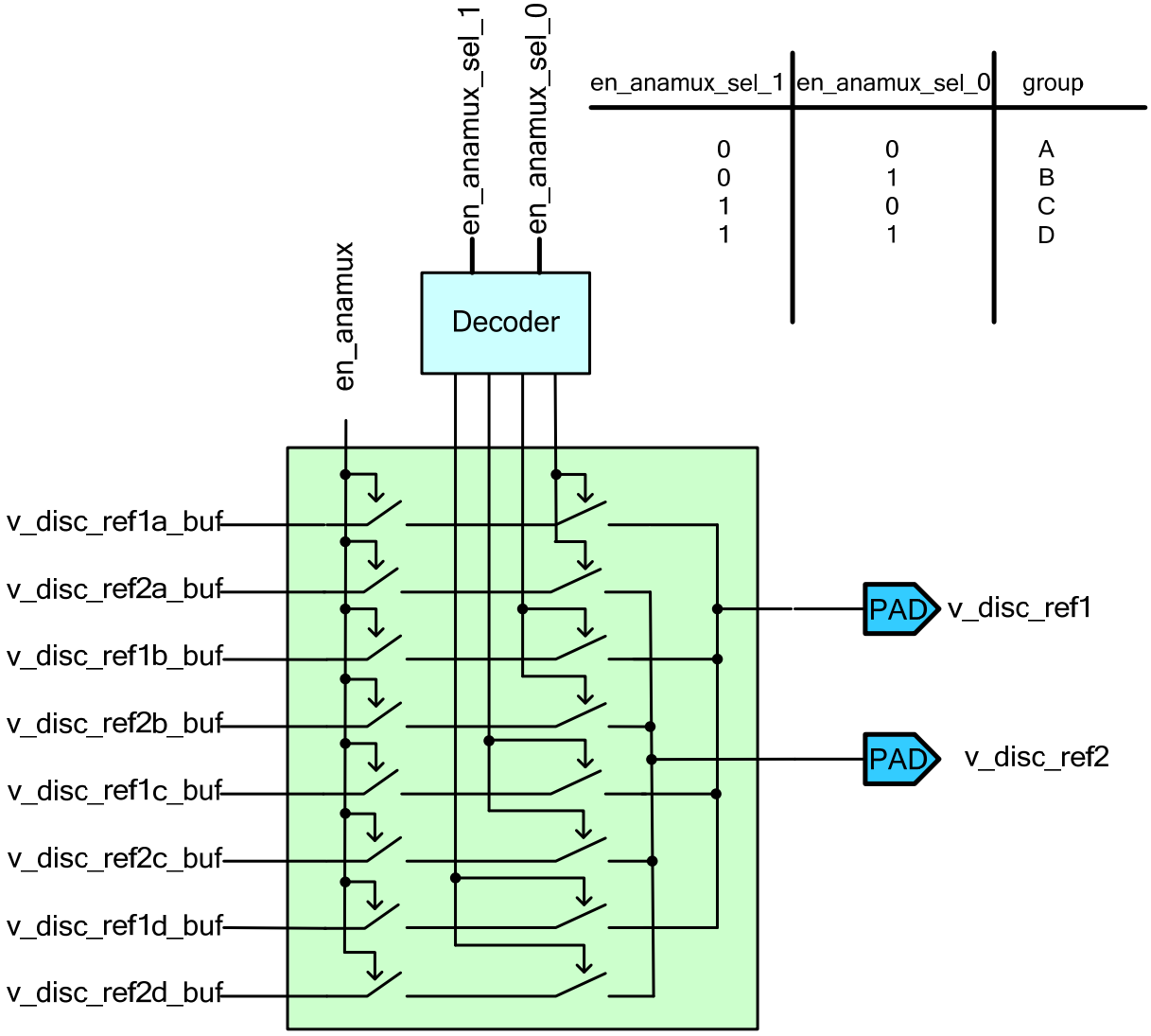
2.5 THE BIAS_GEN Register

The BIAS_GEN register (148 bits wide) sets simultaneously the 19 DAC registers.
After reset the register is set to 0, a value which fixes the minimum power consumption of the circuit. The current values of the DACs are read while the new values are downloaded during the access to the register. An image of the value of some DAC can be measured on its corresponding test pad.

Bit range	N°	Internal Name	purpose	Corresponding Test Pad
147-144	DAC18	v_clp_pix	Pixel clamping voltage	v_clp (1)
143-136	DAC17	i_pix	Pixel source follower bias	
135-128	DAC16	i_disc2	Discriminator bias 2	
127-120	DAC15	i_disc1	Discriminator bias 1	
119-112	DAC14	v_disc_ref2	Discriminator Reference 2	v_disc_ref2 (2)
111-104	DAC13	v_disc_ref1A	Discriminator Reference 1 (Bank A)	v_disc_ref1 (2)
103-96	DAC12	v_disc_ref1B	Discriminator Reference 1 (Bank B)	v_disc_ref1 (2)
95-88	DAC11	v_disc_ref1C	Discriminator Reference 1 (Bank C)	v_disc_ref1 (2)
87-73	DAC10	v_disc_ref1D	Discriminator Reference 1 (Bank D)	v_disc_ref1 (2)
79-72	DAC9	i_ana_buf	Analogue Buffer bias	
71-64	DAC8	v_tst2	Test Level, emulates a pixel output	
63-56	DAC7	v_tst1	IDEM	
55-48	DAC6	i_lvds_rx	LVDS PAD bias	
47-40	DAC5	i_lvds_tx	LVDS PAD bias	
39-32	DAC4	i_disc_pwrs2	Discriminator bias 2 (mode low consp.)	
31-24	DAC3	i_disc_pwrs1	Discriminator bias 1 (mode low consp.)	
23-16	DAC2	i_bufbias	Ref&Tst Buffer bias	
15-8	DAC1	i_pwrs_bias	Discriminator Power Pulse bias	
7-0	DAC0	i_disc_clp	Discriminator Clamping bias	v_disc_clp (3)

(1) The clamping voltage in pixel can be provided either by the 4 bit DAC in the range of 1.9-2.275 V or in an external way (v_clp pads). In this case, the regulator has to be disabled by JTAG access (disvclp).

(2) The voltage v_disc_ref2 are bufferized four times and applied to each group of discriminators A, B, C and D. These four voltages are multiplexed and output on one pad named v_disc_ref2. In the same way, the four voltages v_disc_ref1A, B, C and D are bufferized and applied to each group of discriminators. These four voltages are multiplexed and output on one pad named v_disc_ref1. The group can be selected by JTAG access (en_anamux_sel_1, en_anamux_sel_0). In normal mode, the analog multiplex is disabled (en_anamux = 0).



(3) The voltage v_disc_clp is bufferized and output on the pad named v_disc_clp.

2.6 patt_line0 register

This register “patt_line0” (960 bits large) emulates discriminators outputs. Two registers control the using of the content of this register: en_patt_only and en_linemarker.
With en_patt_only active (high level), the pixel matrix is ignored and replaced by a virtual matrix constituted only of “patt_line0” and”patt_line1”.
This test mode emulates the (digital) pixel response with the contents of the patt_line0 register in order to verify the digital processing. The pattern alternates the contents of the patt_line0 and patt_line1.
In the en_linemarker mode, it adds two rows at the end of matrix for a readout chip. The patt_line0 register is read to emulate the discriminators outputs of these two supplementary rows.
The initialisation phase (reset) presets this register to 0.

Bits range	register name	Purpose	Basic configuration value $Code_{16}$
0-959	patt_line0	Emulate discriminators rows	AAA……..A(1)

(1) Example of pattern used in simulation.

In Ultimate, the patt_line0 <0> is on the left hand side while patt_line0 <959> is on the right hand side.

2.7 dis_disc register

The dis_disc register (960 bits large) disables the discriminator on a specific column, by gating Latch signal and setting the output discriminator at 0.
The default value (0) of the dis_disc register activates all discriminators.
Setting a bit to 1 disables the corresponding discriminator.
In Ultimate, the reading of the discriminator is given from left (dis_disc<0>)to the right (dis_disc<959>).

0 **959 (Msb)**	**(Lsb)**
dis_disc<0>	**dis_disc<959>**

2.8 pix_seq Register

The pix_seq register (112 bits large) contains all parameters to generate readout pixel and discriminator sequence.

Bits range	register name	Purpose	Basic configuration value $Code_{16}$	Signal name
111-96	dsel_row_int	Set reference voltage for diode	ffff	sel_row_int
95-80	dclp	Set reference voltage for clamping	01C0	clp
79-64	dcalib	Sample after clamping	3C00	calib
63-48	drd	Sample before clamping	001C	rd
47-32	dlatch	Latch state of the discriminator	6000 (1)	latch
31-0	dpwr_on	Activate power supply for pixel	ffffffff	pwr_on

After the load of the parameters into the rotate shift register clocked at 80 MHz , each result signal from the table outputs from the last D fliflop. The cycle lasts 16 times clock excepted for the pwr_on.

2.9 Monitoring1 register

The monitoring1 register (30 bits large) gives the setting parameters of the readout controller.

Bit	Register name	Purpose	Basic configuration value $Code_{16}$	
29-20	jtg_sel_rowscan	Row to scan for test.	928 decimal	Normal mode, the number of row matrix is 928.
19-10	jtg_row_mkb	Selection parameter of row for digital marker	002	Digital marker SDS is first row of matrix during the readout
9-0	jtg_row_mka	Selection parameter of row for analogue marker	0001	analogue marker SDS is first row of matrix during the readout

2.10 patt_line1 Register

The patt_line1 register (960 bits large) emulates discriminators outputs rows in *en_linemarker* and en_patt_only modes.

When en_patt_only is active, the values stored in the pixel matrix are ignored and the value of patt_line1 is sent to the discriminators outputs. This is a test mode which emulates the (digital) pixel response with the contents programmed into the patt_line0 register in order to verify the digital processing. The pattern is alternated with the contents of the patt_line1.

In the en_linemarker mode, it adds two rows at the end of matrix for a readout chip and the patt_line1 register is read to emulate the discriminators outputs of these two supplementary rows.

Bit range	register name	Purpose	Basic configuration value $Code_{16}$
0-959	patt_line1	Emulate discriminators rows	5555……..55555(1)

(1) Example of pattern used in simulation.

In Ultimate, the patt_line1 <0> is on the left hand side while patt_line1 <959> is on the right hand side.

With patt_line1 together these two signals will form the elements of the simulated frame given to SUZE part.

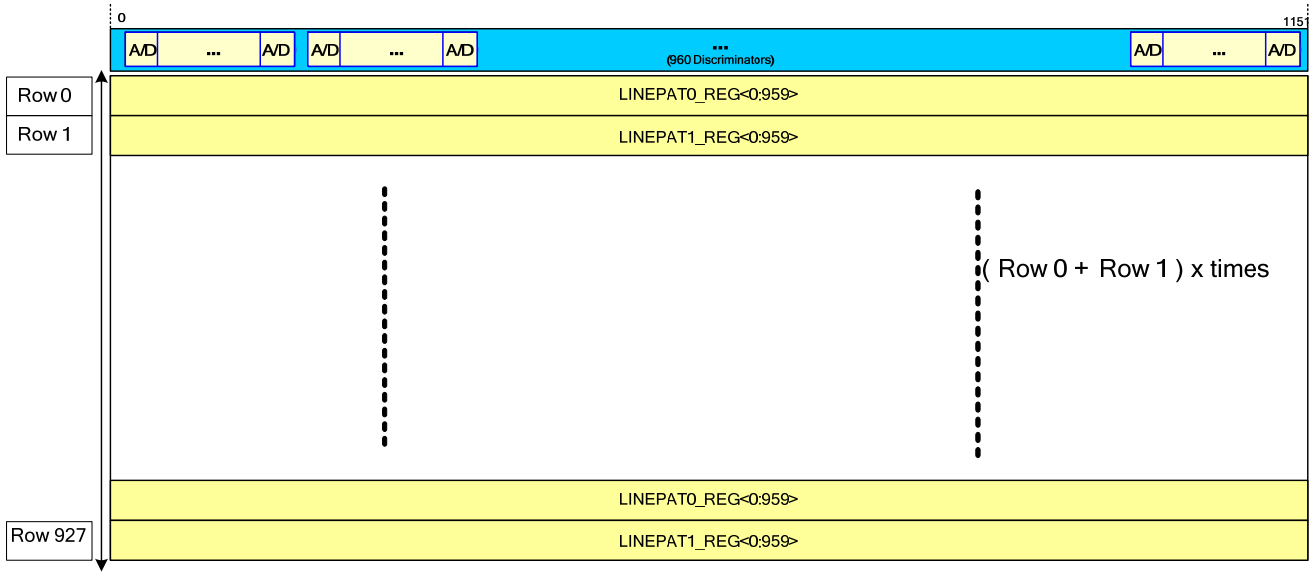


Figure 16 : Generation of the test frame pattern

2.11 suze_seq register

The suze_seq registers (160 bits large) contains all parameters to generate readout zero suppression (suze) sequence.

Bit range	register name	Purpose	Basic configuration value $Code_{16}$	Signal Name
159-144	dckrdpixmux	Sample signal for multiplexer after SDS	0555	ckrdpixmux
143-128	dcklatch	Synchronization signal every line for SDS	3000	cklatch
127-112	dcklatchmem	Synchronization signal every line for memory management	1000	cklatchmem
111-96	dckmemlatch	Synchronization signal every line for SDS	0555	ckmemlatch
95-80	dckrdpix5ns	Synchronization signal 6 times every line for memory management shifted of 5 ns compared with Ckrdpix	82aa	ckrdpix5ns
79-64	dckrdpix	Synchronization signal 6 times every line for memory management	0555	ckrdpix
63-48	dstartline	Synchronization signal every line for memory management	e001	startline
47-32	drstline	Synchronization signal every line for all SUZE part	6000	rstline
31-16	drstpix	Reset signal 6 times every line for SDS	0555	rstpix
15-0	drstframe	Reset frame signal for memory management	2000	rstframe

- Related timing with f_{clk}=80 MHz (Theses signals are used by zero suppression circuit).

2.12 header_trailer register

The register called header_trailer includes 4 registers of 16 bits as shown below.

Bit range	Bit Name	Purpose	Basic configuration value	
63-48	header0	Synchronization header for serial output0	5555	
47-32	header1	Synchronization header for serial output1	5555	
31-16	trailer0	Synchronization trailer serial output0	AAAA	
15-0	trailer1	Synchronization trailer serial output1	AAAA	

For both modes according to the register DUALCHANNEL the header and the trailer of each data frame can be different. The following table shows the possible *Header* and the *Trailer* which ensure the unicity in the data frame. The unicity is guaranteed without the *Frame counter*.

Bits	0-3 (in hexa)	4-13	14	15
Possible Header or Trailer	1	X	1	X
	2	X	1	X
	3	X	1	X
	4	X	1	X
	5	X	1	X
	6	X	1	X
	7	X	1	X
	8	X	1	X
	A	X	1	X
	B	X	1	X
	C	X	1	X
	D	X	1	X
	E	X	1	X
	F	X	1	X

Table 1: possible *Header* and *Trailer* for mode 0 and 1 to ensure unicity (or mode 2 with 32 bits)

2.13 Monitor 2 Register

The Monitor2 register (8 bits large) allows setting parameters of the test pads.

Bit range	Bit Name	Purpose	Basic configuration value $Code_{16}$	
7 - 4	Sel_tstpad1	Selection of the synchronization signal on test pad1	0	
3 – 0	Sel_tstpad2	Selection of the synchronization signal on test pad2	0	

The internal following signals can be selected with SelPad1 and SelPad2 (4 bits).

Cfg multiplexors configuration

This configuration register selects the output signals on the external pads.
The following tables describe the different capabilities.

SelPad1	Tst1Pad	Purpose
0	MK_Test_D	Digital marker corresponding to last serialized digital data. It depends of RowMkd selection parameter.
1	pwr_ons	Same signal as PwOn, but shifted of 16 main clock
2	pwr_on	Activate power supply for pixel
3	sel_row_int	Connect pixel output to common column
4	clp	Set reference voltage for clamping
5	gnd	
6	rd	Sample before clamping
7	calib	Sample after clamping
8	mk_test_a	Analogue marker is shifted of 80 ns to MK_A signal. This signal rises up at the beginning of the reading phase and falls down at the end of Calib phase. It depends of RowMka selection parameter
9	mk_rd	Analogue marker corresponding to Rd phase of readout pixel. It depends of RowMka selection parameter
10	mk_calib	Analogue marker corresponding to Calib phase of readout pixel. It depends of RowMka selection parameter
11	ckdivx2	Clock divided by 2
12	mk_a	Analogue marker corresponding to readout pixel sequence. It depends of RowMka selection parameter.
13	latch	Latch state of the discriminator
14	+ vdd	
15	Gnd	

SelPad2	Tst2Pad	Purpose
0	cklatch	cf. suze_seq §
1	cklatchmem	cf. suze_seq §
2	ckmemlatch	cf. suze_seq §
3	ckrdpix	cf. suze_seq §
4	ckrdpix5ns	cf. suze_seq §
5	ckrdpixmux	cf. suze_seq §
6	latch	cf. suze_seq §
7	clkdiv8	Main Clock devided by 16
8	startline	cf. suze_seq §
9	rstline	cf. suze_seq §
10	startframe	cf. suze_seq §
11	rstframe	cf. suze_seq §
12	clp	
13	rstpix	
14	synmux	
15	seqrstb	

Figure 17: Cfg multiplexors configuration

2.14 RO_MODE4 Register

Bit range	register Name	Purpose	Rst status	configuration value
7	Not used			
6	dis_pstart	Disable the start pad	0	0
5	dis_pspeak	disable the speak pad	0	0
4	dis_ppll	Disable the pll pad	0	0
3	dis_pdo1	Disable the D1 pad	0	0
2	dis_pdo0	Disable the D1 pad	0	0
1	dis_mkd	Disable the marker pad	0	0
0	dis_pclkd	Disable the clkd pad	0	0

2.15 RO_MODE3 Register

Bit range	Register name	Purpose	Rst status	configuration value
7	en_anamux_sel_0	Select the group of discriminators for the reference voltages (A,B,C or D)	0	0
6	en_anamux_sel_1	IDEM	0	0
5	en_anamux	Enable the analog multiplexor	0	1
4	en_rd_delay	Enable the delay for reading	0	1
3	dis_vclppix	Disable the internal clamping voltage for pixel	0	0
2	en_cfg_cmdgen	Enable the command generation configuration	0	1
1	clkrateout	Determines the clock rate of the outputs channel or in one channel	0	1
0	dualchannelout	Determines the data stream on the channel or in one channel	0	1

Data stream output

Clkrateout	Dualchannelout	Cfg	Description	
0	0	0	The data are sampled by the frequency output clock 80 MHz.	The data stream is output on data line 1 only, Data line 0 stay to low level
0	1	1		The data stream is output on both data line 0 and 1.
1	0	2	The data are sampled by the frequency output clock 160 MHz.	The data stream is output on data line 1 only, Data line 0 stay to low level
1	1	3		The data stream is output on both data line 0 and 1.

2.16 RO_MODE2 Register

Bit range	Register name	Purpose	Rst status	Basic configuration value
7	en_tstpad	Enable the pad test	0	0
6	en_disc_line	enable the line discriminator	0	0
5	en_gateckmod	Gating clock mode ON/Off	0	0
4	Not used		0	0
3	en_aftermuxtst	Enable mode scan test for multiplexer of suze	0	0
2	en_disc_d_tst	Enable mode scan test discriminators	0	0
1	en_scan	Enable mode scan test	0	0
0	en_disc_autoscan	Enable mode scan test discriminators, all matrix	0	0

2.17 RO_MODE1 Register

The RO_MODE1 registers (8 bits large) allow selecting specific analogue mode of the chip.

Bit range	Bit Name	Purpose	Rst status	Basic configuration value
7	en_startframe	Reinitializes the frame counter to 0.	0	0
6	en_ana_tst	Enable the 8 columns at right of the matrix for the analog outputs	0	0
5	en_anadriver_scan	Enable scan pixel mode	0	0
4	dis_bufref	Disable the reference buffers	0	0
3	en_pll	Use the PLL clock as main clock	0	0
2	en_disc_aop	Enable the power pulse amplifier	0	0
1	en_disc_pwrsave	Enable the discriminator power pulse mode	0	0
0	en_disc_tst	Enable the discriminator test mode	0	0

2.18 RO_MODE0 Register

The RO_MODE0 registers (8 bits large) allow the user to select specific digital mode of the chip.

Bit range	Register name	Purpose	Rst status	Working mode
7	en_v_disc_digtst	Enable the internal injection of VTEST	0	0
6	en_sel8outs	Enable the 8 columns in the middle of the matrix for the analog outputs	0	0
5	dis_lvds	Disable the input LVDS clock and active clock CMOS.	0	0
4	en_linemarker	Add two rows at the end of matrix for the chip readout: The LINEPAT_REG register is selected to emulate discriminators outputs. For analogue outputs, the 2 Test Levels, VTEST1 and VTEST2 are selected which emulate a pixel output in RD and CALIB phases.	0	0
3	en_mode_speak	Select Marker signal or Readout Clock for digital and analogue data (MK_CLKA and MK_CLKD pads)	0	1
2	en_patt_only	Test Mode: Select LINEPAT_REG to emulate discriminators outputs	0	0
1	en_extstart	Enable external START input synchronization (1)	0	1
0	en_start_jtag	Enable JTAG START input synchronization (2)	0	0

(1) The minimum wide of asynchronous external START signal is 500 ns the maximum 1 µs, and this signal is active at high level.

(2) When en_extstart is disabled, it's possible to generate internal START by accessing JTAG_Start bit. JTAG_Start signal is realized by three JTAG access: First step, this bit is set to 0, second step it is set to 1, and at last it is set to 0.

2.19 BYPASS Register

The Bypass register consists of a single bit scan register. Its selection loads the code in the Instruction register: during this load the instruction register contains an undefined instruction.

3 Running Ultimate

The following steps describe how to operate Ultimate

3.1 Reset initialization

3.1.1 Introduction

The asynchronous reset (rstb power reset) controls all the parts of chip including the configuration (slow control by JTAG).
A start signal independently of this signal generates an internal synchronous reset without modifying the configuration.(No slow control reset)

3.1.2 Sequence

The sequence is the following one:
a) Power supply switch on: Vdd
b) power reset signal coming (asynchronous reset),
c) supply of the clock clk_cmos or clk_lvds.
g) internal synchronous reset generation

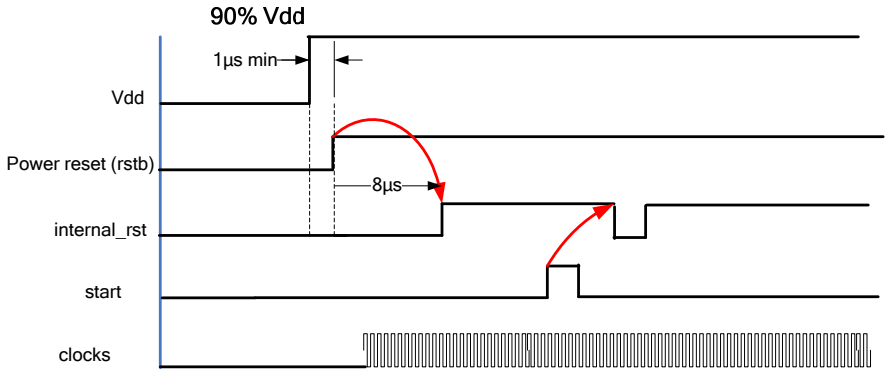


Figure 18: timing diagram of the reset sequence

3.2 After reset

On RSTB active low signal:

- All BIAS registers are set to the default value, i.e. 0
- dis_disc is set to 0, i.e. all columns are selected,
- ro_mode0, ro_mode1, ro_mode2, ro_mode3, ro_mode4 are set to 0
- pix_seq is set to 0,
- pix_seq is set to 0,
- seq_suze is set to 0,
- header_trailer is set to 0,
- patt_line0 is set to 0,
- patt_line1 is set to 0,
- monitoring1 and monitoring2 are set to 0,
- JTAG state machine is in the Test-Logic-Reset state
- JTAG ID_CODE instruction is selected

Then the initial sequence controls the load of the bias register and all the previously quoted registers are set in the running conditions. According to the settings, the readout can be performed either in normal mode or in test mode.

3.3 Setting the bias_gen register

The BIAS_GEN register must be loaded before operating Ultimate.
For biasing the Ultimate chip, there are 18 DACs building with the same current mode 8 bits DAC (1 µA of resolution) and 1 specific 4 bits DAC for setting the pixel clamping voltage. Interfaces as current mirrors for current sourcing or sinking, resistors or current-voltage converter circuit customize each bias output.
The following table shows the downloaded codes which set the nominal bias.

Internal DAC Name	Simulation			Resolution	Range
	$Code_{16}$ – $Code_{10}$	Dac Internal current-µA	Output value		
VPIXCLP	0-0		1.9 V	25 mV	From 1.9 V to 2.275 V
IPIX	32-50	50	50 µA	1 µA	From 0 up to 255 µA
IDIS2	20-32	32	5 µA	156 nA	From 0 up to 255 µA
IDIS1	20-32	32	10 µA	312 nA	From 0 up to 255 µA
IVDISREF2	76-118	100	1.01 V	10 mV	From 1 up to 1.5 V
IVDISREF1A	80-128	128	1.01 V	250 µV	From -32 up to 32 mV (1)
IVDISREF1B	80-128	128	1.01 V	250 µV	From -32 up to 32 mV (1)
IVDISREF1C	80-128	128	1.01 V	250 µV	From -32 up to 32 mV (1)
IVDISREF1D	80-128	128	1.01 V	250 µV	From -32 up to 32 mV (1)
IAnaBUF	32-50	50	500 µA	10 µA	From 0 up to 255 µA
IVTEST2	76-118	100	1.01 V	10 mV	From 1 up to 1.5 V
IVTEST1	80-128	128	1.01 V	250 µV	From -32 up to 32 mV (1)
ILVDSRX	20-32	32	7 µA	218 nA	From 0 up to 255 µA
ILVDSTX	28-40	40	40 µA	1 µA	From 0 up to 255 µA
IDis2PwrS	A-10	10	100 nA	10 nA	From 0 up to 255 µA
IDis1PwrS	A-10	10	100 nA	10 nA	From 0 up to 255 µA
IBufBias	A-10	10	10 µA	1 µA	From 0 up to 255 µA
IPwrSWBias	A-10	10	10 µA	1 µA	From 0 up to 255 µA
IVDISCLP	64-100	100	2.1 V	10 mV	From 1.2 up to 3.2 V

(1) Referenced with respect to IVDREF2. The threshold voltage of the discriminators ΔVth is defined as Vref1-Vref2 (Vref1=Vref2+ΔVth).

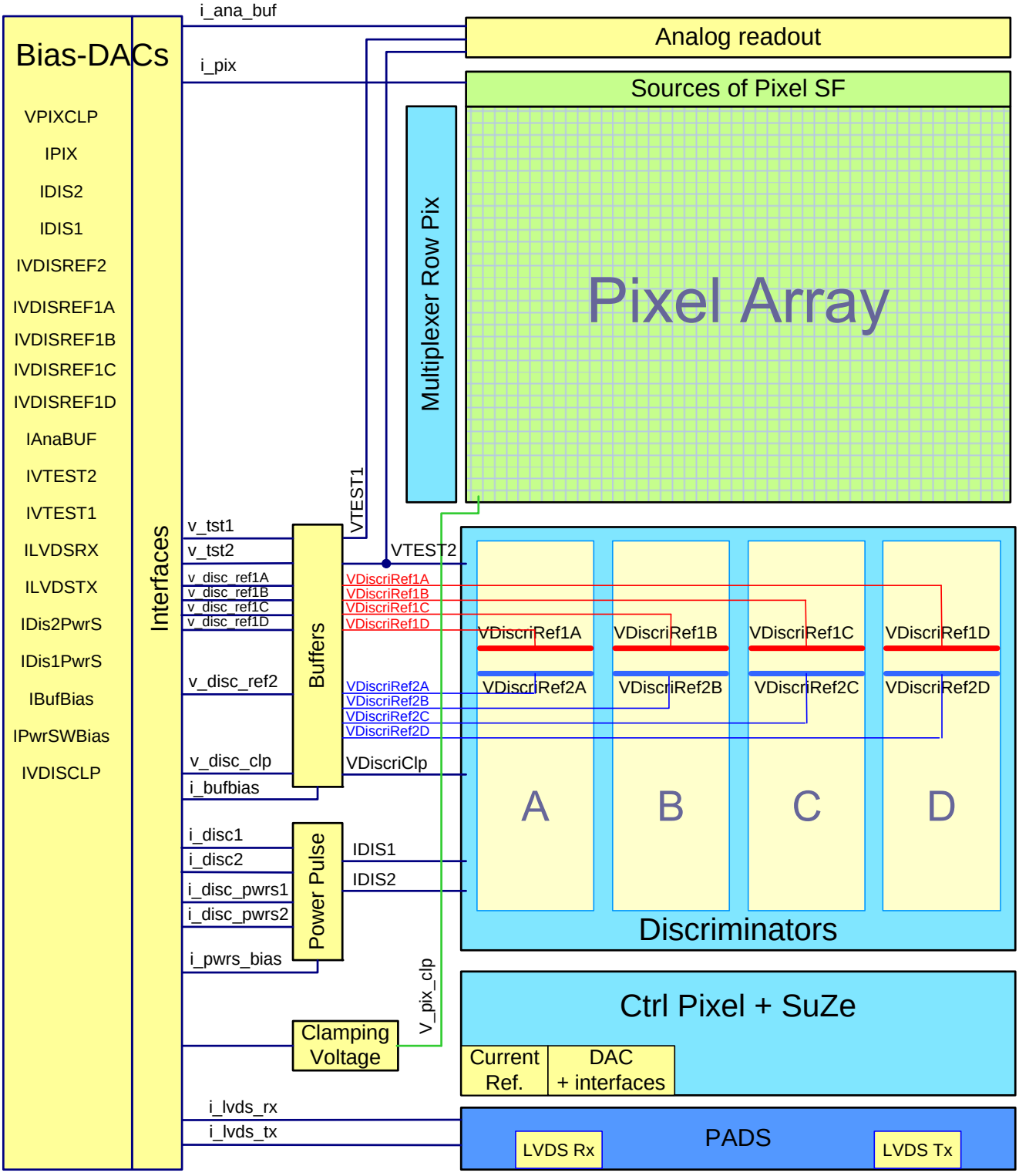


Figure 19: Bias synthetic bank diagram

3.4 Analogue and digital Data Format

3.4.1 Main Introduction

The analogue outputs, dedicated for test purpose offer two kinds of output signals:

- pixel signals,
- synchronization signals.

For digital outputs, the IC generates two types of signals:

- digital pixel signal after zero suppression processing
- test discriminator and test zero suppression logic:

  - Digital pixel signal by discriminator
  - Test pattern used by zero suppression logic, reading the LINEPAT_REG register

Ultimate uses the pads at the bottom edge for all its operations, whatever is collecting data from the pixels (using the pixels and the discriminators) or in test mode (reproducing at the outputs the pre-programmed patterns). All the digital signals to synchronize and programming the chip are necessary to operate successfully.
Analog outputs located on the top edge of the chip are not used for the normal operations. The main purpose is to characterize the pixels or to check the dead pixels. Therefore measurements on these pads deal with normal pixel signals as well as test signals (but they still require the synchronization and the markers) and it is activated on demand by setting to 1 the en_ana_tst bit in the RO_MODE1 register.

3.4.2 Normal mode data format

3.4.2.1 Introduction

This chip includes the main features of Mimosa 26. The inputs are the main clock, the reset and an input synchronization signal (START) for initializing the readout control.

The sparsified output data of the previous frame are sent during the acquisition of the current frame.

The data of SUZE are serialized on two output pads and two other signals are provided for the DAQ:

- A clock (clkd),
- Two data lines (pad_do0 and pad_do1), and
- A marker (mkd).

The serial output has four configuration modes according to 2 registers *clkrate* and *dualchannel* (see §2.3.12 as shown later). **All the words (16 bits) are read from the LSB to the MSB**.

The different part of the data frame is the *Header*, *Frame counter*, *Data Length*, *States/Line*, *State*, and *Trailer*.

The 2 words elements (ie *Header*, *Frame counter*, *Data Length* and *Trailer)* are divided into two parts. For instance, the header includes Header0 (corresponds to the 16 bits LSB) and header1 (corresponds to the 16 bits MSB).

The *Header*, the *Trailer* and the *Marker* signal could be used together to detect loss of synchronization.

3.4.2.2 The Clock

The clock is always present even if the data transmission is finished. Its rate depends on the clkrate register. 160 MHz or 80 MHz

3.4.2.3 Marker

The marker (mkd) is available in all modes. The *Marker* signal set to one during 4 clock's rising edges can also be used to detect the beginning of a data transmission.

3.4.2.4 Header trailer

The *Header* and the *Trailer* composed of 2 x 16 bits (header0 –header1),(trailer0 –trailer1) allow the detection of the beginning and the end of a data transmission respectively.. The *Header* and the *Trailer* are totally configurable by JTAG (the header and the trailer can be different). The Table 1 (see §2.3.11) shows the possible *Header* and *Trailer* values.

3.4.2.5 Frame counter

Frame counter is the number of frames since the chip was reset. This counter (32 bits) is reset to 0 when the maximum is reached (FFFFFFFF in hexadecimal) and continues to work. The JTAG register startframe receives successively to 1 and 0 reinitializing the counter to 0.

The *Frame counter* when separated into 2 words is given in the *Data line 0* (*Frame counter 0*) with the LSB's and in the *Data line 1* (*Frame counter 1*) the MSB's.

3.4.2.6 Data Length

Data Length is the number of word of 16 bits of the useful data. *Data Length* is written on 32 bits. In the case of one data line, the number of words is repeated 2 times. The sum determines the real value of the useful data

In the case of no hit during a frame, *Data Length 0* and *Data Length 1* are set to zero.

3.4.2.7 Useful data (*States/Line, State)*

The useful data is the daisy chain of *States/Line* and *States.*

The maximum number of the useful data bits sent during one frame is (1850 words of 32 bits) 59200 bits.

In some rare case, the number of data generated by the suppression of zeros exceeds the maximum bits capable to be sent, thus the data frame will be truncated.

The data are periodically sent at the beginning of each new frame. The number of bits sent between two headers is variable and depends on the numbers of the words recorded during the last frame.

Each data lines have the same number of bits. Consequently *Data Length 0* and *Data Length 1* are the same.

States/Line and *State* have exactly the same meaning whatever the selected mode.

The number of words sent in a data frame depends of the number of hits. If the number of words for the two data lines is even, the last *Status* of *Data line 1* is false. This operating way allows having the same number of bits (Data length) in the both *DO0 and DO1* in every case. This false *Status* can be detect by the last *Status/Line*, because the number of *State* sent is one more than the *Status/Line* expected.

States/Line contains the address of the hit line, and the number of *State* for this line (between one and nine) and an overflow flag.

The following table describes the signification of the bits in *Status/Line* word.

Status/ line															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit(0-3)				Bit(0-9)											
number of *States*				The address of the line										Not used	OVF

Table 2 : Description of *States/line* word

State contains the address of the first hit pixel and the number of successive hit pixels as shown on the table below.

State															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit(0 -1)		Bit(0-9)													
number of hit pixels		the address of the column										not used			

Table 3 : Description of *State* word

The table below resumes the **maximum** length of the output frame according to the selected mode.

Clk rate out	Dual channel out	Config.	Out	Header	Cptframe	Datalength	Number of useful data (words of 16 bits)	trailer	Total words	Nb of empty words
0	0	0	D00	Unused = 0						
			D01	Header0 & Header1	Cptframe0 & Cptframe1	Datalength0 & Datalength1	459 + 459	Trailer0 & Trailer1	924	4
0	1	1	D00	Header0	Cptframe0	Datalength0	918	Trailer0	926	2
			D01	Header1	Cptframe1	Datalength1	918	Trailer1	926	2
1	0	2	D00	Unused = 0						
			D01	Header0 & Header1	Cptframe0 & Cptframe1	Datalength0 & Datalength1	922 + 922	Trailer0 & Trailer1	1852	4
1	1	3	D00	Header0	Cptframe0	Datalength0	1850	Trailer0	1854	2
			D01	Header1	Cptframe1	Datalength1	1850	Trailer1	1854	2

The figure below describes the format of data send by Ultimate in the one data line mode.

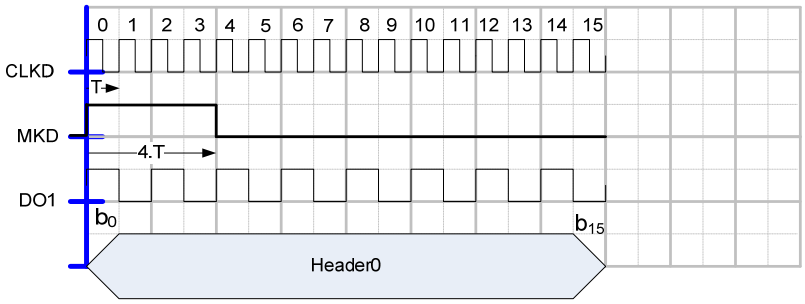


Figure 20: Detail of the beginning of a data frame

Mode 80 MHz Mono channel (*clkrate= 0* and *dualchannel = 0)*

The maximum number of data generated by the suppression of zeros is (459 x 2 x 16) bits for the output.
This overflow implies the truncation of the data frame.
This mode 0 giving too little information (thus irrelevant) can be used as test only.

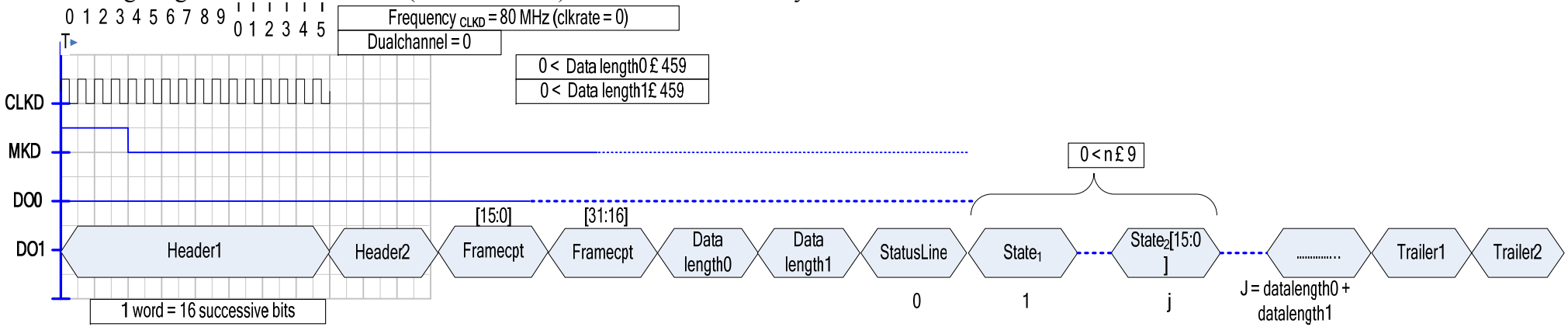


Figure 21: Format of the output Data of Ultimate Mono Channel and 80 MHz

Mode 80 MHz Dua
l channel (*clkrate= 0* and *dualchannel = 1)*

The maximum number of data generated by the suppression of zeros is (918 x 16) bits for each output.
This overflow implies the truncation of the data frame.

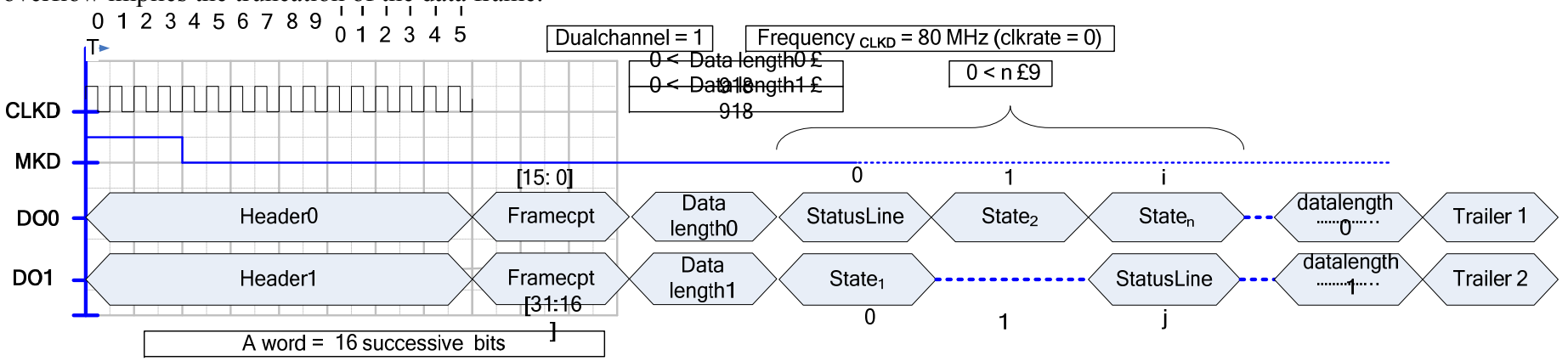


Figure 22: Format of the output Data of Ultimate Dual Channel and 80 MHz

Mode 160 MHz Mono channel (*clkrate= 1* and *dualchannel = 0)*

The maximum number of data generated by the suppression of zeros is (922 x 2 x 16) bits for the output.
This overflow implies the truncation of the data frame.

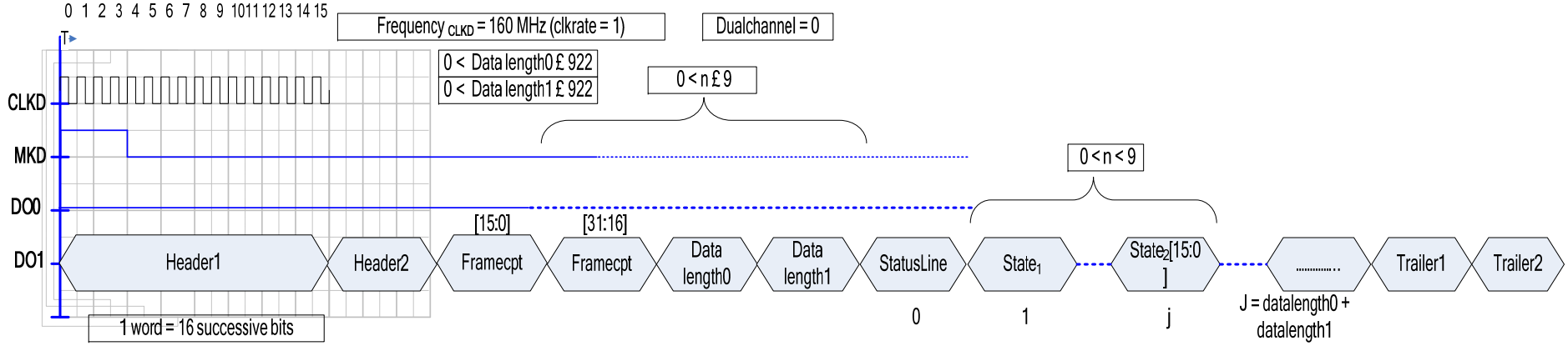


Figure 23: Format of the output Data of Ultimate Mono Channel and 160 MHz

Mode 160 MHz dualchannel (*clkrate= 1* and *dualchannel = 1)*

The maximum number of data generated by the suppression of zeros is (1850 x 16) bits for each output.
This overflow implies the truncation of the data frame.

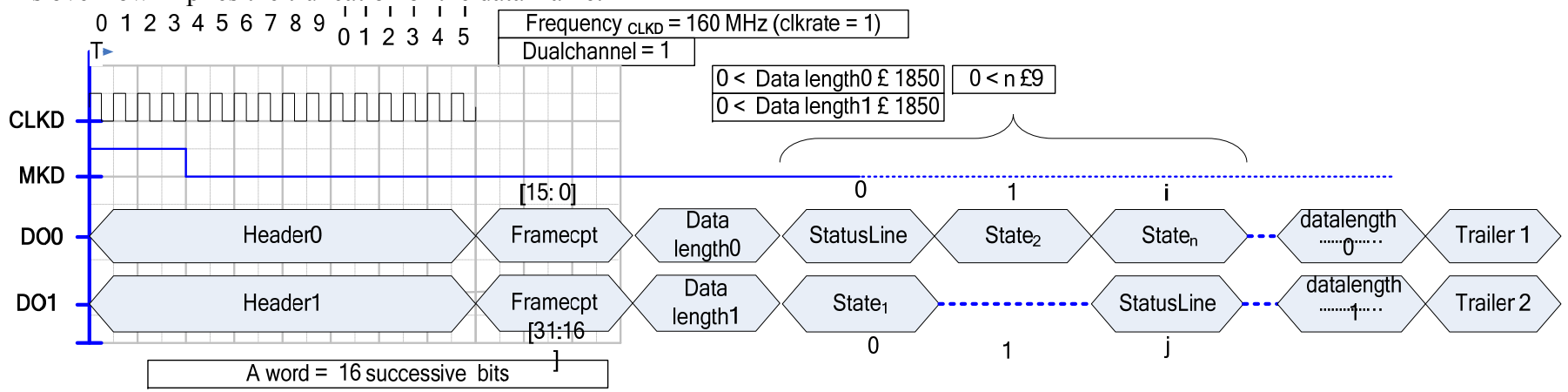


Figure 24: Format of the output data: **Mode 160 MHz dual channel**

3.4.3 Test mode

3.4.3.1 Analogue outputs, Normal pixel signal

The en_ana_tst bit set to '1' in the RO_MODE1 register implies the connection of the rightmost 8 columns of pixels to the 8 voltage buffers, the outcoming signals are available on output pads at the top of the matrix . The en_anadriver_scan set to '1' starts the analog test, in the RO_MODE1. The scanning of the matrix now starts and stripes of 8 pixels are connected to the analog outputs. The analog test is performed considering a reduced size of the array (about 928 rows x 8 columns), it requires therefore acquisitions of 120 frames to analyze the full matrix. The next figure shows how to realize the analog characterization and which parts of the matrix are under test for each frame.

The MKA is the synchronization marker for the analog outputs. When "en_ana_tst" bit set to '1', it appears at the end of each frame, sampling the analog channel of the new frame on the next rising edge of CLKA.

Further with "en_anadriver_scan" set to '1', this marker appears at the end of the frame for each sub matrix.

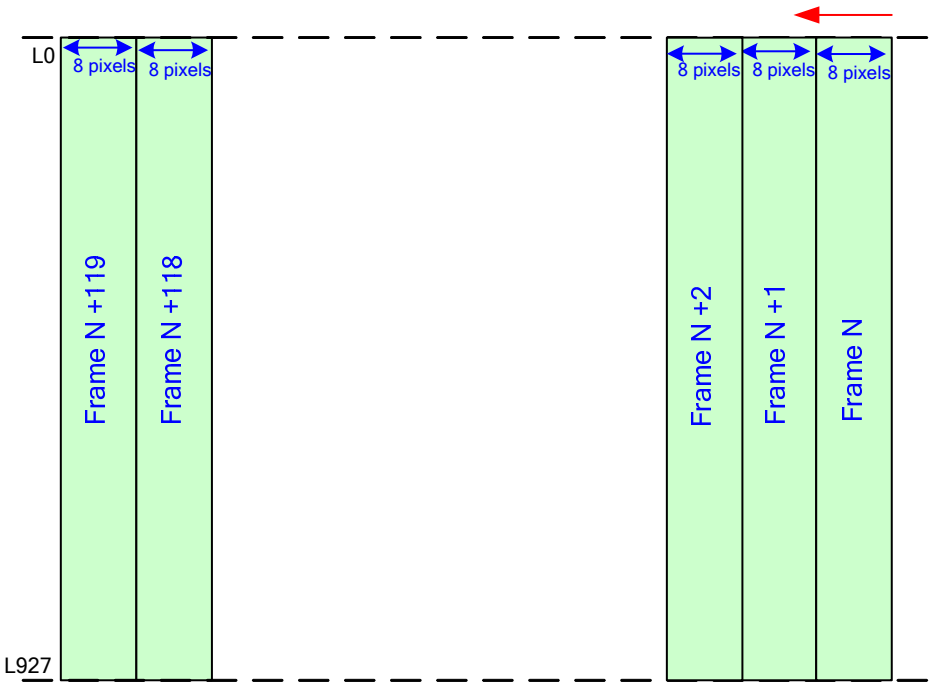


Figure 25: Analog characterization of the pixel

The matrix of pixels divided in stripes of 8 columns is fully scanned at each frame, and then swapped with the next block of 8 columns at right and so on until the complete analyze of all the columns.

Figure 26 Mode scan for analog output

3.4.4 Transfer function of discriminator and pixel digital readout calibration

3.4.4.1 Introduction

This test readout mode allows obtaining the transfer function of discriminator and calibrating the digital readout (Pixel + discriminator).

3.4.4.2 Transfer function of discriminator:

During the test mode (*en_disc_tst* bit set to '1' in the RO_MODE2 register), the pixel matrix is not connected to the discriminators. Only one test level Vtest2 is applied to the discriminator input to emulate pixel base line.
The DAC offers the possibility of adjustment of this voltage. The Vtest2 voltage is chosen closed to the VDISREF2 voltage.
The VDISREF1 voltage scan allows performing the transfer function of the discriminator. There are 4 DACs corresponding to the four banks of discriminators (A, B, C and D).

3.4.4.3 Pixel digital readout calibration:

During the test mode (*en_disc_d_tst* bit set to '0' in the RO_MODE1 register), the pixels are connected to the discriminators.
This mode allows obtaining pixel digital readout calibration.

During one frame, one row is processed and the outputs of discriminators are serialized with falling edge of CLKD (CLKL/8) and send off chip via DO0 and DO1 pads. The synchronisation marker for digital data outputs on MKD pad and corresponds to first bit serialized.

The pixel array calibration can be realized in automatic mode (when *En_disc_autoscan* is set to 1, §RO_MODE2 Register).
In this mode, the scanning of the pixel array takes 928 frames long (One frame per line).

3.4.4.4 Synoptic

According to the synoptic, the scanning of the whole line (960 bits) outputs from one shift register of 512 bits and one of 448 wide.

3.4.4.5 Transfer function of discriminator and pixel digital readout calibration

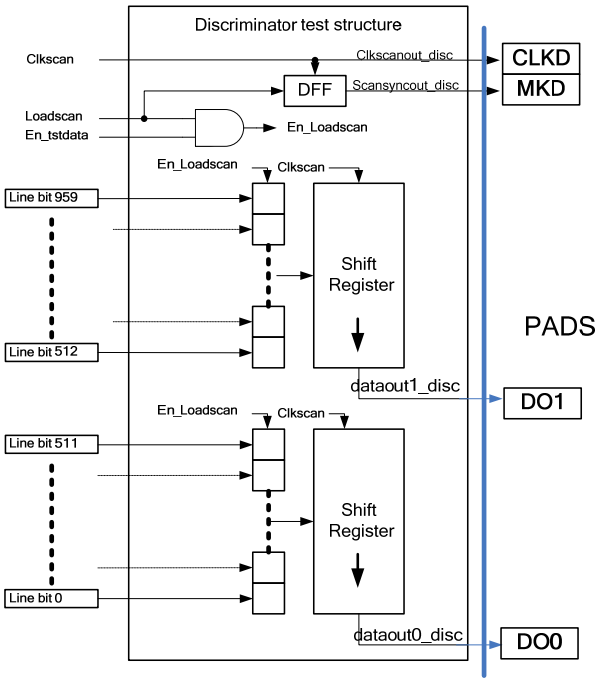


Figure 27: discriminator test block diagram

3.4.4.6 Timing diagram

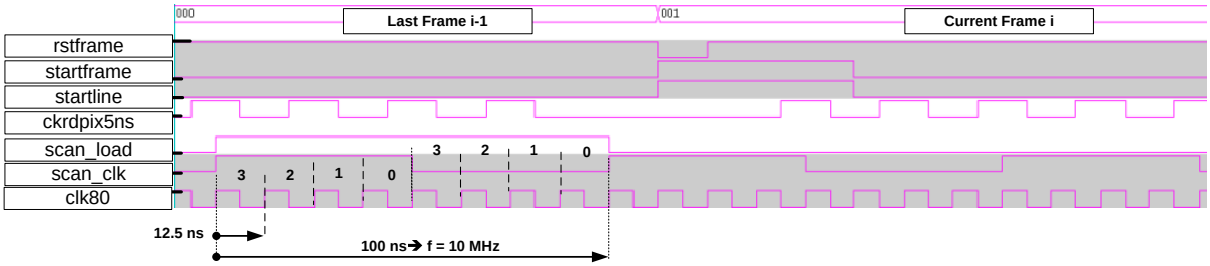


Figure 28: Start of scan load and scan_clk

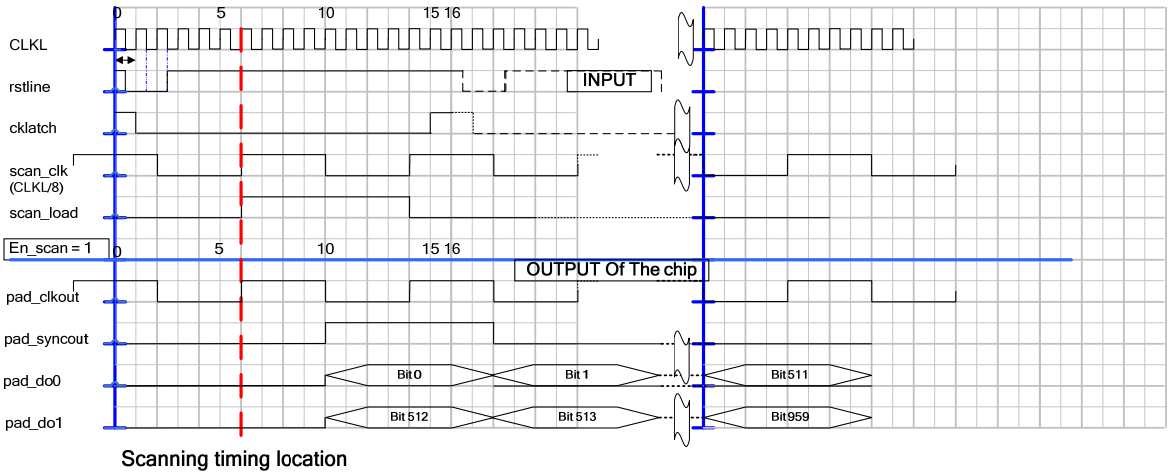


Figure 29: Sequence of the line reading

The jtg_sel_rowscan of the monitor1 Register gives the row address into the frame.

For both modes, the table below shows the following bits of the ro_mode2 registers:

Bit Name	Value configuration
en_scan	1
en_aftermuxtst	0
en_disc_d_tst	1

Two modes are defined:

- When en_disc_autoscan is set to 0, we select one row defined into jtg_sel_rowscan (0 to 927). When this mode is started, at each frame, the selected row is scanned (the readout process is continuous). To change the row address, we define other scan line into jtg_sel_rowscan and generate a new START signal.
- When en_disc_autoscan is set to 1, we select the row automatic scanning (from line 0 to 927) and the process stops when last row is scanned (see the Figure below), *but line 0 and line 511 are not scanned*.

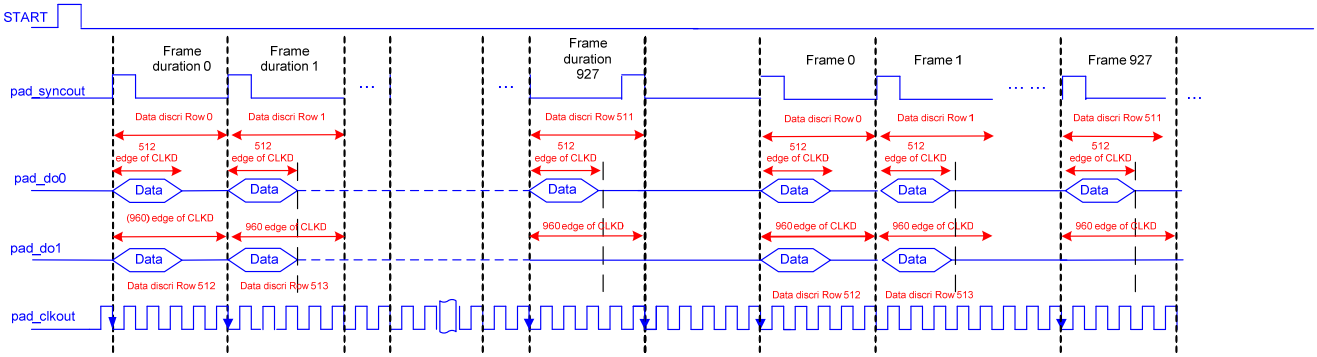


Figure 30: scanning automatic test of the Data discriminator (en_disc_autoscan = 1)

3.4.5 SUZE multiplexer test

3.4.5.1 Introduction

The SDS results are combined by a multiplexer. This test allows validating the multiplexer.
To realize this test, we emulate inside the chip a matrix of 960 rows. For this purpose, the patt_line0 and patt_line1 must be used as exSDSined on paragraphs §2.3.5 and §2.3.9. We select one address row defined into jtg_sel_rowscan(0 to 23F) of the "suze_seq" register. During each frame, the selected row is processed and the data outputs after multiplexer (data frame is 160 bits wide) are serialized with falling edge of CLKD (CLKL/8) and transmit off chip via DO0 pad (DO1 pad is not used). The synchronisation marker for digital outputs is generated on MKD pad and corresponds to first bit serialized.

3.4.5.2 Configuration test

Register	Bit Name	Value configuration
suze_seq	En_scan	1
	En_auto_scan_discri	0
	Test_after_mux	1
ro_mode0	En_patt_only	1
patt_line0	959-0	User defined.
patt_line1	959-0	User defined same as patt_line0 to simplify the checking of this test

3.4.5.3 Synoptic

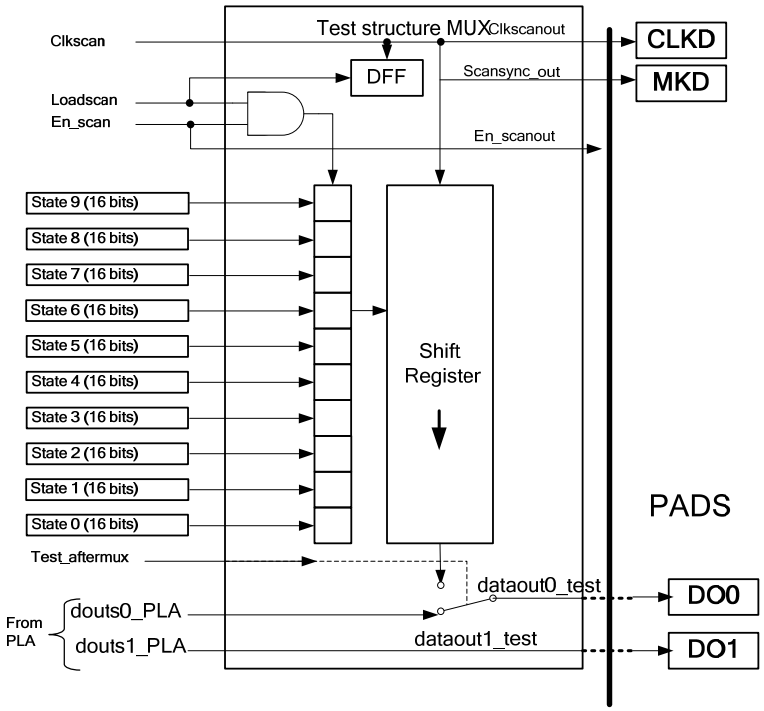


Figure 31: MUX test structure block diagram

3.4.5.4 MUX scanning word description

The first bit outputting from the shift register is the LSB of the word (160 bits) analyzed as following.

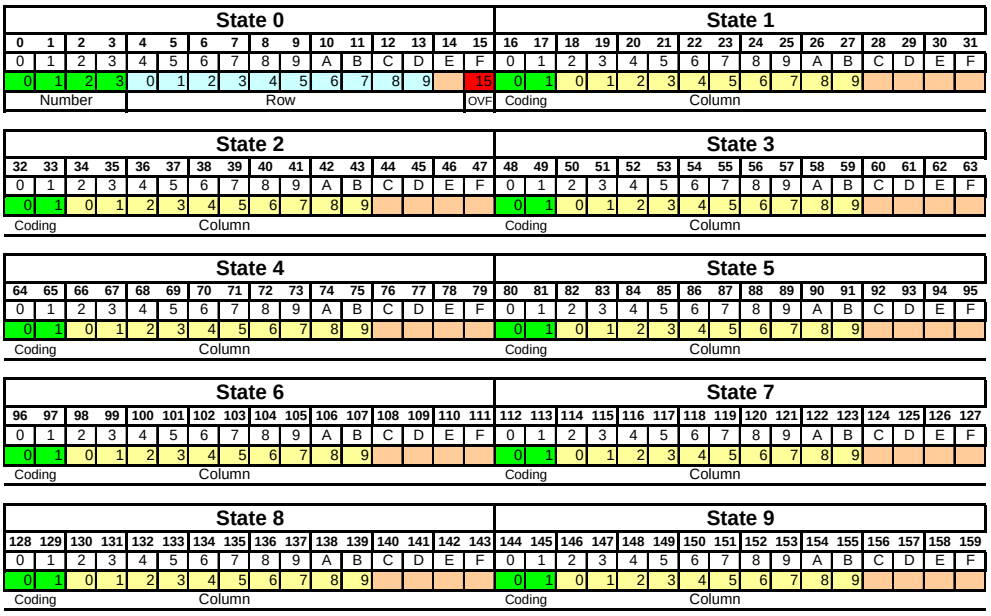


Figure 32: Format of the MUX word Test

Caution:

The following range of bits unused (29:31), (45:47) (61:63) (77:79) (93:95) (109:111) (125:127) (141:143) (157:159) are **undefined**.

3.5 Main sequencer

3.5.1 Introduction

After the power external reset, and after the configuration of the JTAG registers, the external user sends a start sequence. The unit first generates an internal low active reset "seqrstb_a"(or seqrstb_d), and starts all the internal finite states machines (fsm) for the schedule and the synchronization of ultimate chip. All internal functions are set to the initial states, and the internals registers receives the values from JTAG.

If the desired operating mode does not correspond to the default one, set all configuration registers following to the appropriate settings cf. configuration registers in annex §JTAG Register Set .

For main synchronization signals, we use the following process:

- At the reset mode, the value of each parameter is latched on a shift register.
- At the working mode, this shift register works as a circular shift register (looped on itself).

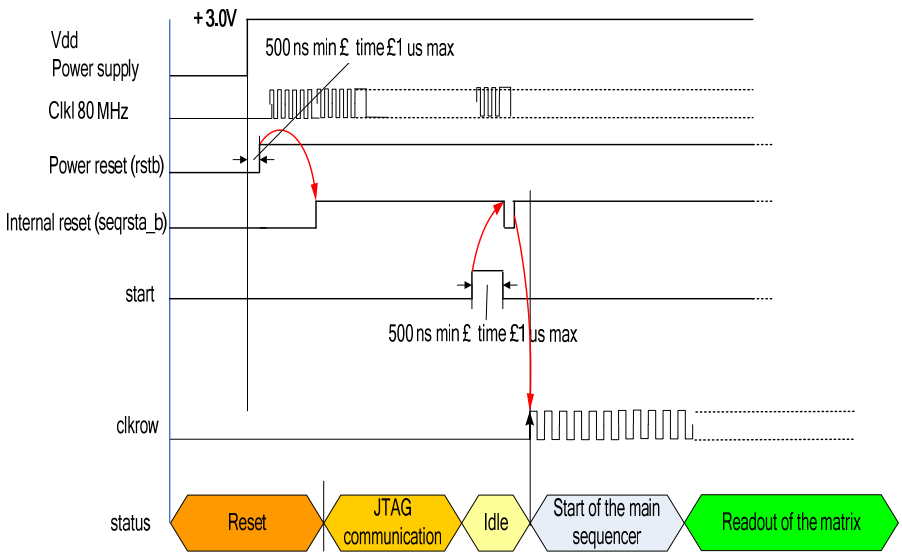
For a signal synchronized

- On a line, the cycle takes 16 times clock.
- On a frame, the cycle takes 928 x one line time.

$$time\_clock = \frac{1}{80\,MHz} = 12{,}5ns$$

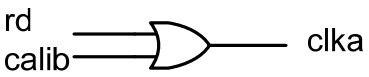
3.5.2 Main phases for ultimate

After the loading of the JTAG registers, the readout of Ultimate can initiated with the following sequence:



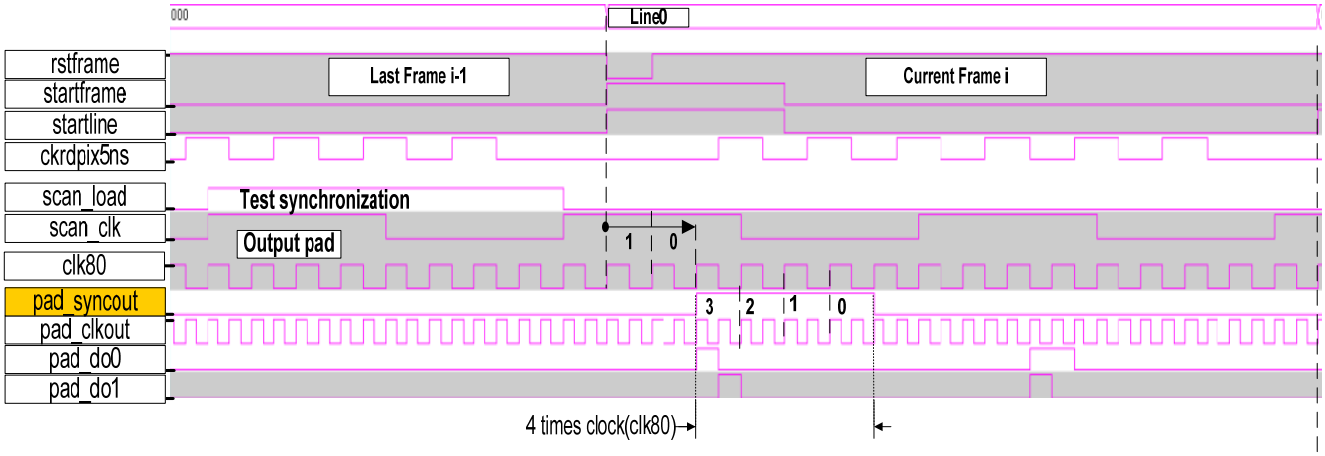
Signal markers allow the readout monitoring and the data outputs (analogue and digital) sampling:

- "clka and clka_mk are running when the main sequencer starts.



- When “speak” signal is active, marker of synchronization for analogue outputs is generated on “clka_mk” pad.

- Marker of synchronization for digital outputs is generated on “pad_syncout”, this signal is shifted of 2 times clock (clk80) from “startframe” signal, “pad_syncout” is set during 4 times ”clk80” independently of the signal “speak”.



3.5.3 Synchronization for stop and re-start readout

Successive pixel frames are read until the readout clock is stopped.
A frame resynchronization can be performed at any time by setting up the “start” token again.

3.5.4 Chronograms for a the first frame readout

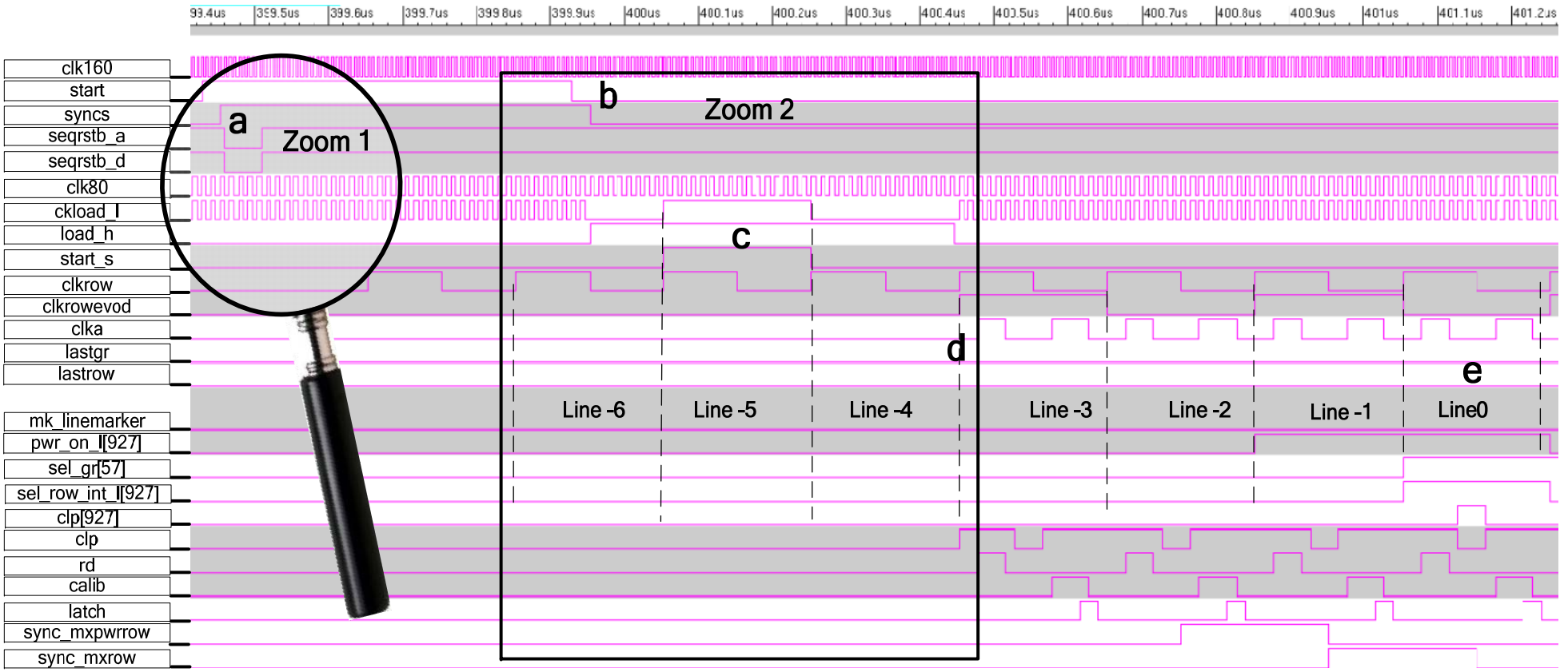


Figure 33: readout start initial phase

a) After 2 rising edge of the clkl when start = 1, the internal seqrstb_a and seqrstb_d are generated.

b) After the falling edge of START signal, when the first falling edge of clkrow, the sequence of sequencer_pix_reg is actived for state machine Readout Controller when load_h is staying at the high level,

c) The data sequencer_suze_reg is loaded to a state machine Readout Controller during line-5 phase.

d) At the falling edge of "load_h", the sequencer "fsm for pixel" generates all useful signals for pixel and discriminators

e) The readout of the matrix starts.

starts.

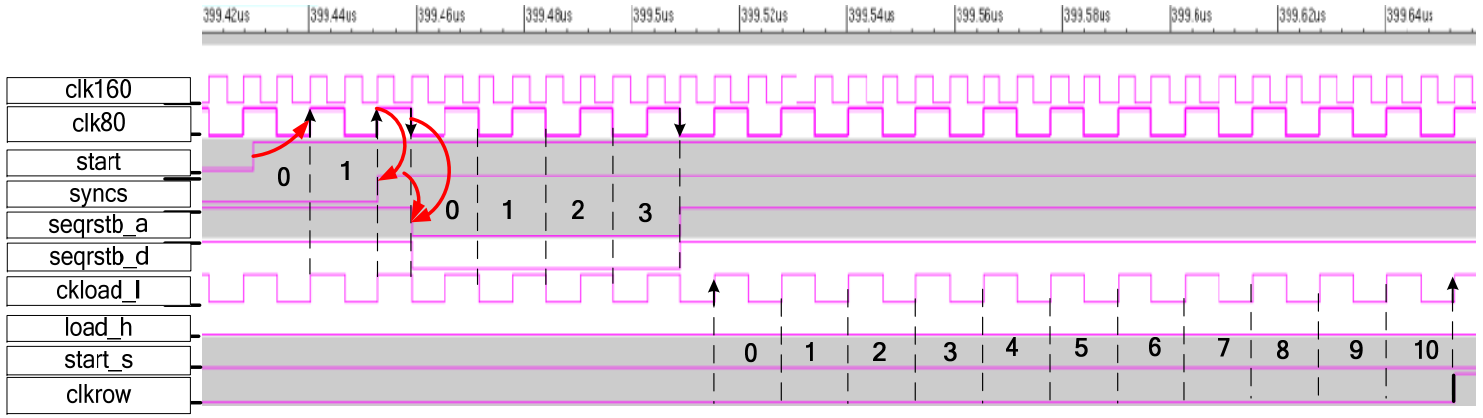


Figure 34: zoom 1 on the readout synchronization of the internal reset

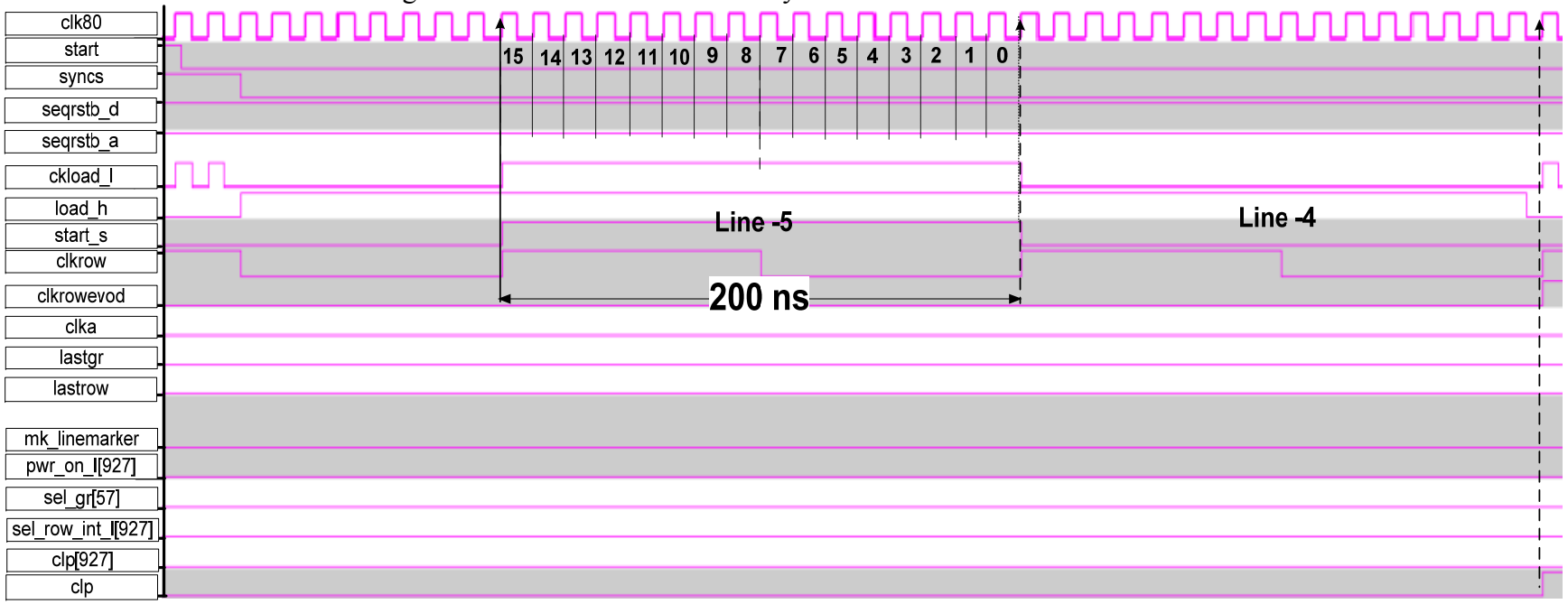


Figure 35: zoom on the readout clock row and latency before read-out

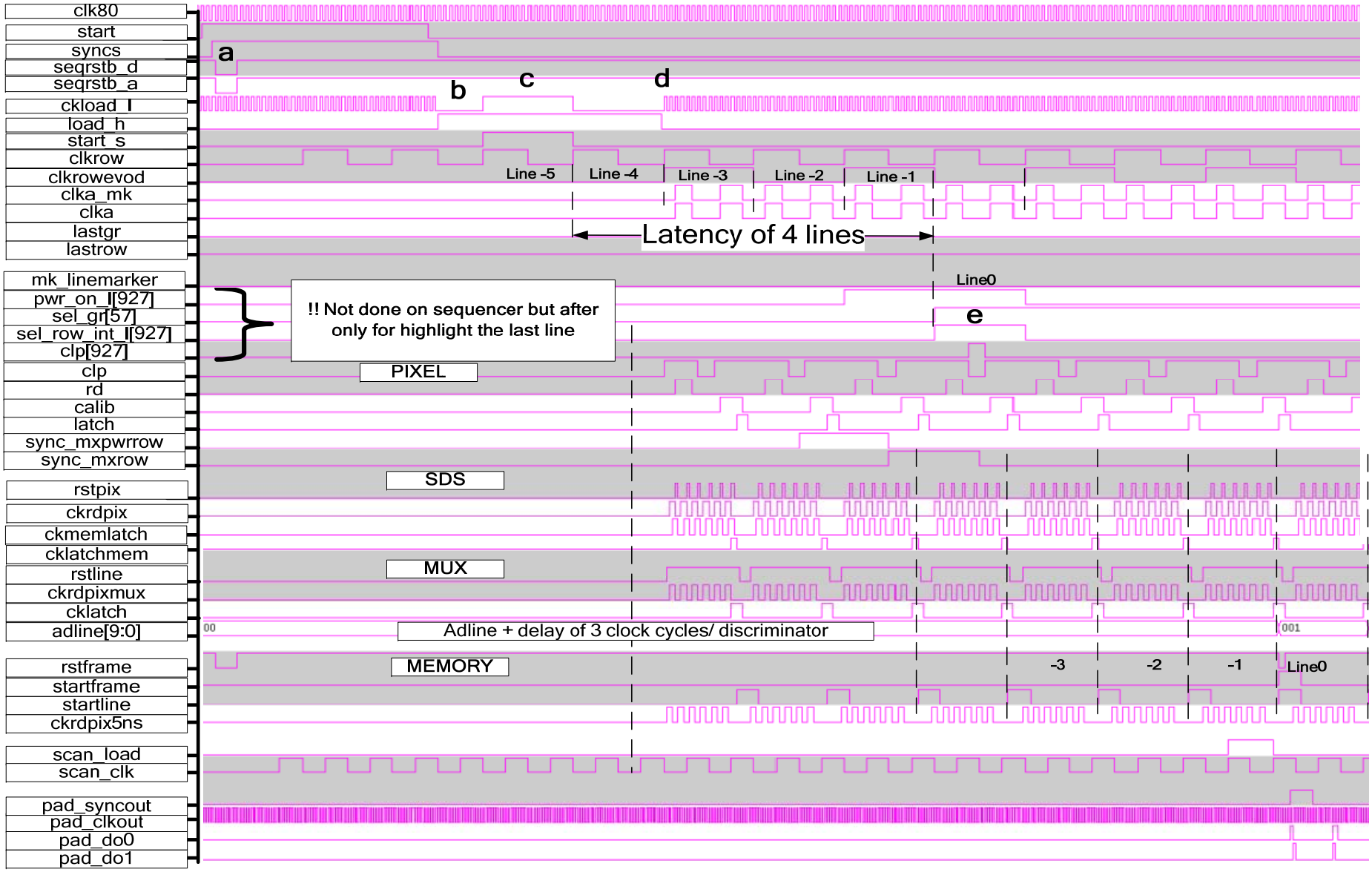


Figure 36: Pipeline of the readout processing from analog to memory part simulation timing diagram

3.5.5 Line synchronization for pixel and discriminator

The sequencer generates the signals for all lines. A block below will distribute them for each line independently. Cf. § Pixel and discriminator read out sequence synchronization
For the configuration registers see §pix_seq Register

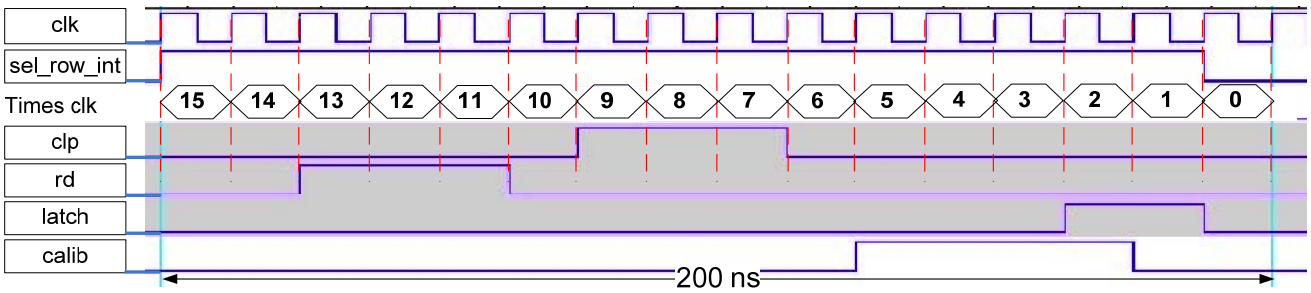


Figure 37 : Simulation timing diagram for the pixel part

Related timing with f_{clk}=80 MHz (rd, calib, latch signals are used by the column readout circuitry).

3.5.6 Line synchronization for suze

The picture below resumes the synchronization signals used for all suze part, output of the discriminator, sds, mux and memory management for each line.

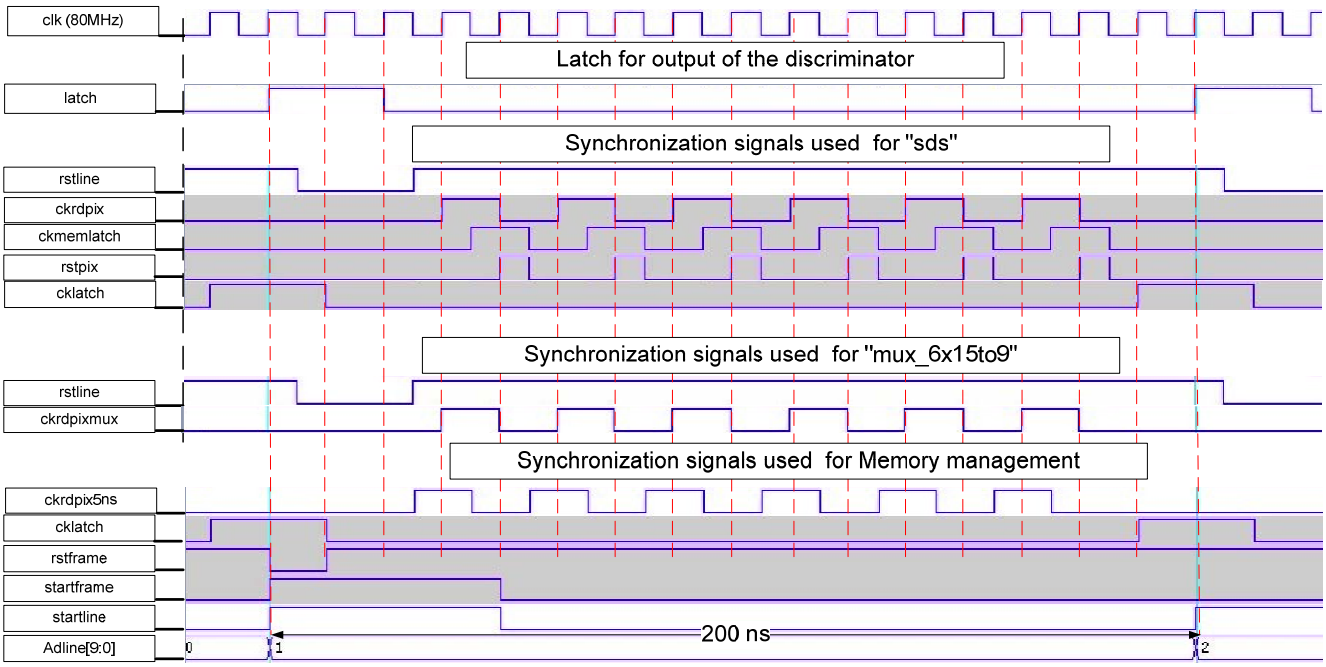


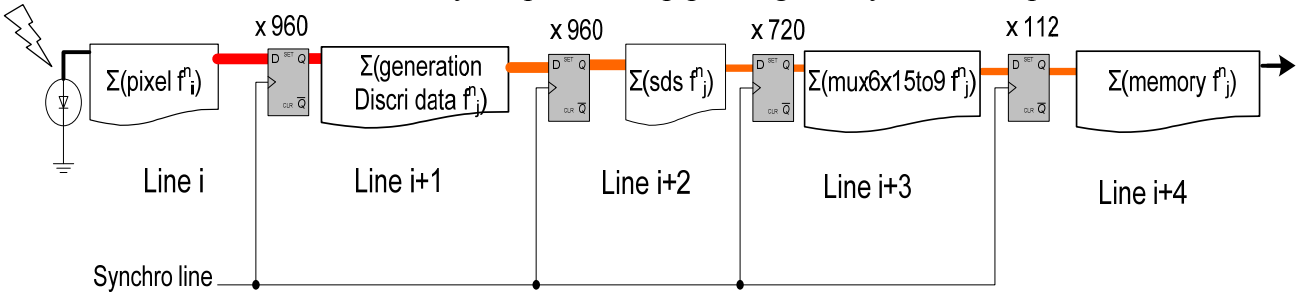
Figure 38: synchronization periodic signals for “suze” part

3.5.7 Pipeline of the readout chain

Each stage of the chip is complex from analogical acquisition (pixel) to the storage of the pixel data and requires time for achievement of all function.
The operation of each block lasts one line time (given by the following equation).

$$\boldsymbol{linetime} = 16 \times \frac{1}{80\boldsymbol{MHz}} = 200\boldsymbol{ns}$$

The schematic below shows very simplified the pipeline given by the main operations.



We introduce a margin of minimum 10 ns between the end of the achievement of the functions and the rising edge of the synchronization line of each stage to increase the reliability of the readout.
The chip switches 2752 latch boxes (960 +960+720+112) at the same time. With the experience on Mimosa26 and the separation of the analog and digital supply voltages, the experiment shows that these switches present low influence and do not disturb the pixel stage.

3.6 Pixel and analog core sequencer

3.6.1 Pixel and discriminator read out sequence synchronization

The digital core realizes the switching sequence for the matrix of pixels and the discriminators.
The following succinct synoptic illustrates where the signals act during the line in each pixel of the row and one discriminator per column in the matrix.
The pwr_on is activated when the start signal (high level) is sent to the chip and stays at the high level.

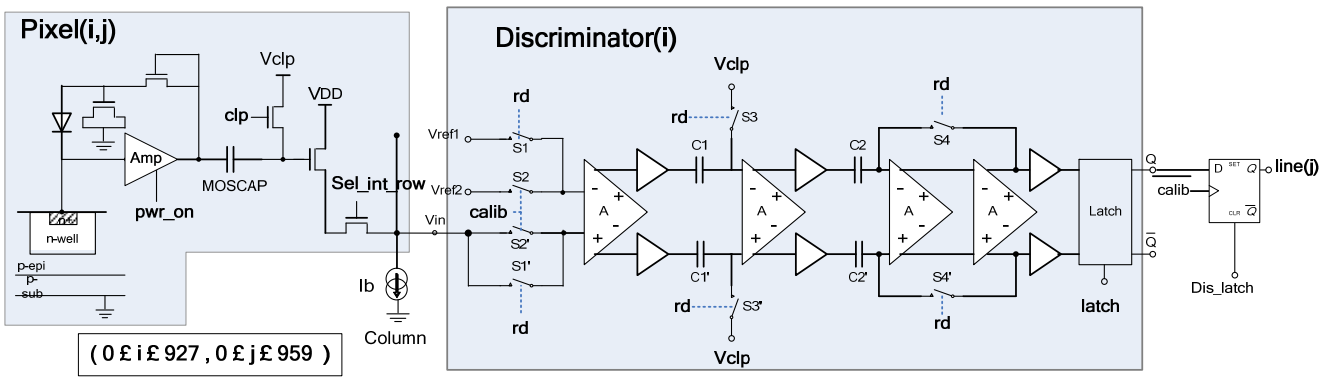


Figure 39: pixel and discriminator synchronization structure

The following picture represents the cycle of one row of 960 pixels. That means that 960 pixels are sampled at the same time then 960 discriminators works in parallel at the same time.

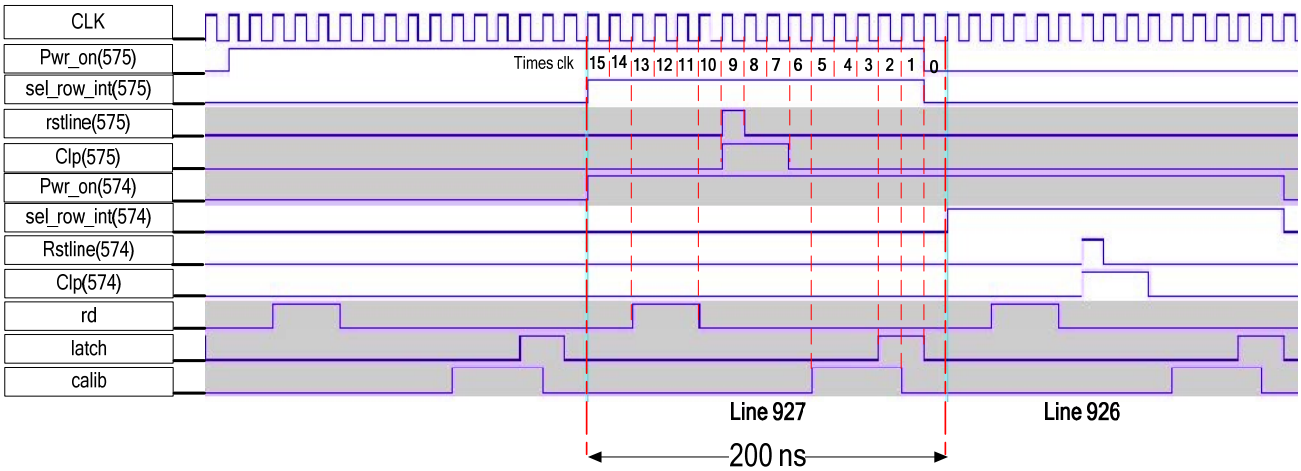


Figure 40: the cycle of one row of 960 pixels and discriminators

For the whole matrix the schematic below shows the switching applied to the pixel into the row and into the lines.

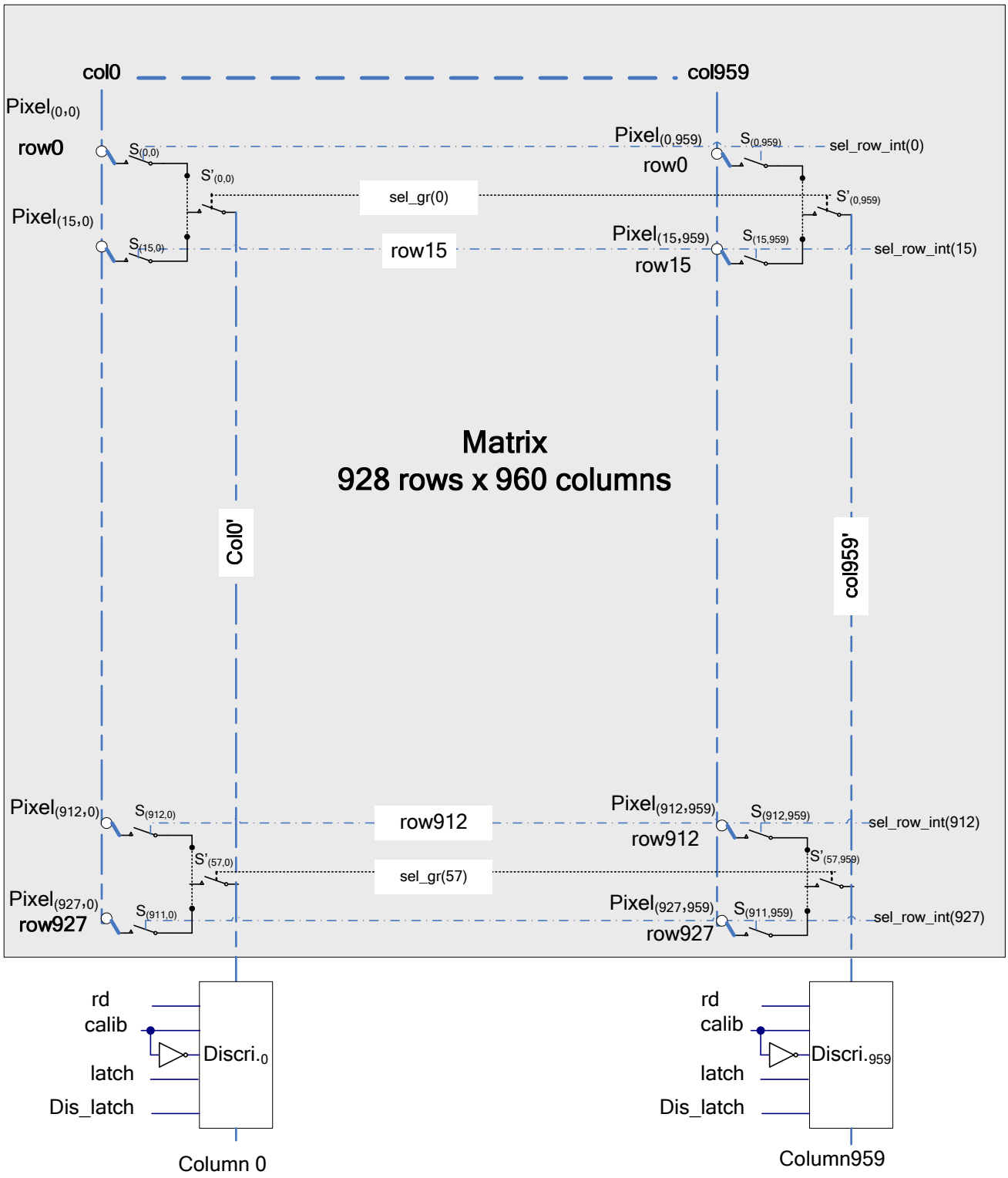


Figure 41: matrix of pixels and discriminators for switching

The following picture shows the initialization phase of the synchronizations signal applied to the discriminator.

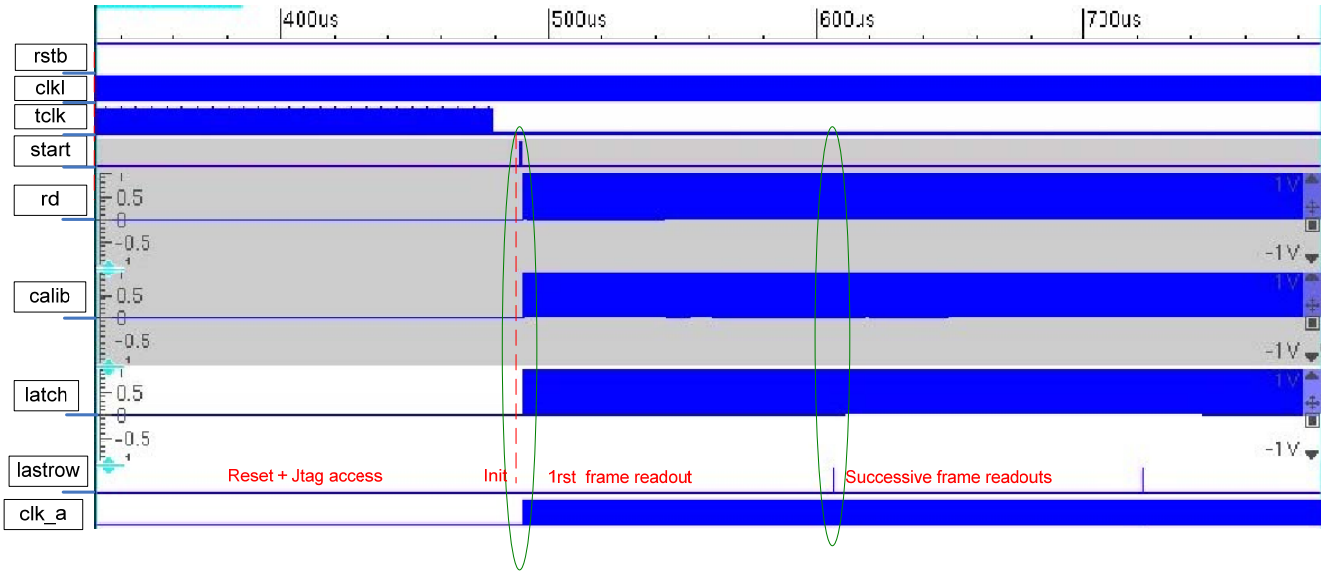


Figure 42: matrix of pixels and discriminators

The following pictures show the synchronization signal for the readout of the matrix, note the generation of the different clock like clkrow (frequency line), clkrowevod (frequency every 2 lines) and the clp (one per line) (clamping of the pixel frequency).

Figure 43: timing diagram after the start matrix of pixels and discriminators frame 0

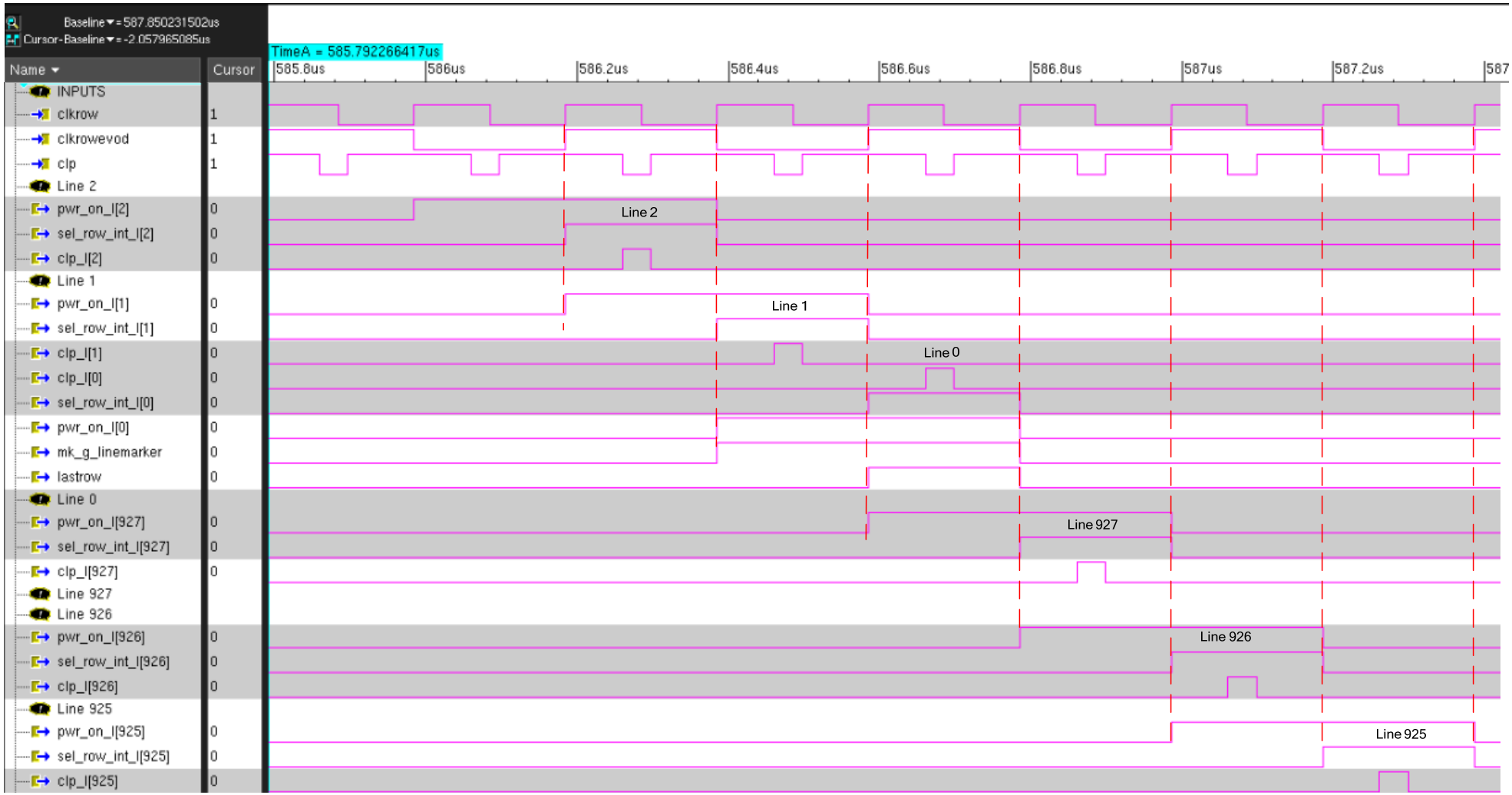


Figure 44: timing diagram after the start matrix of pixels and discriminators others successive frames

3.6.2 Disable discriminator output sequence

The ASIC offers the possibility to disable one or several discriminators outputs by a configurable register of 960 bits. Cf. §2.7 dis_disc register
The change can be done each new JTAG and start sequence.

3.6.3 Analog discriminators sequence test

This block is only used for test and calibration. Cf. annex § 2.18 RO_MODE0 Register

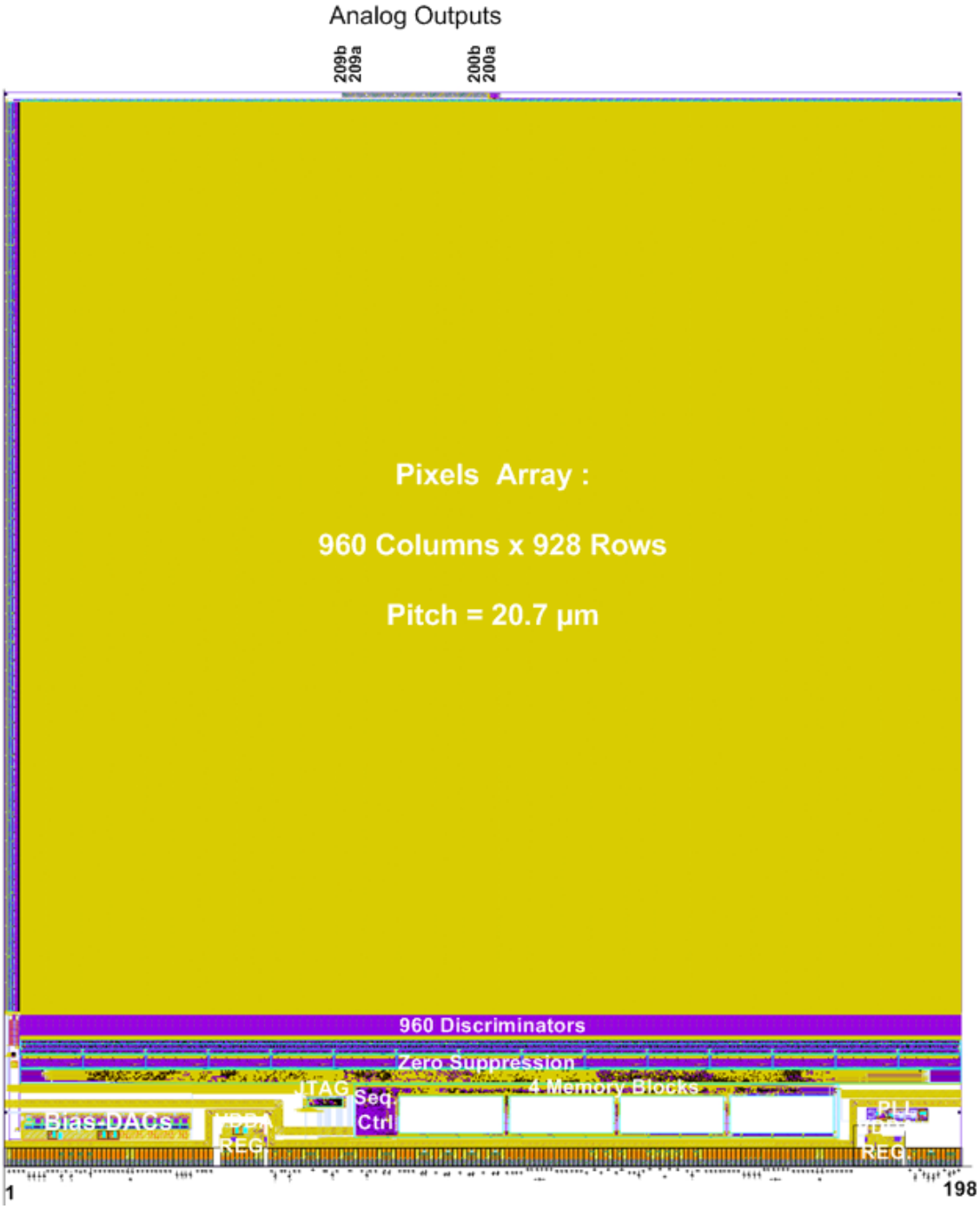
3.7 Main Signal Specifications

	Parameter	Typical Value	Notes
INIT	RSTB Pulse Width	>1 µs	Active Low, Asynchronous Power on Reset
JTAG	TCK Frequency	10 MHz	Boundary Scan Clock
	TMS Setup/Hold Time	~10 ns	Boundary Scan Control Signal
	TDI Setup/Hold Time	~10 ns	Boundary Scan Serial Data In
READOUT	CKRD Frequency	Up to 160 MHz	Readout Clock LVDS signal
	CKRD Duty Cycle	50%	
	SYNC Setup/Hold Time	5 ns	Chip initialisation, CMOS signal. Starts after falling edge on 1rst CKRD sampling

3.8 Pad Ring

The pad ring of Ultimate is built with

- Pads full custom designed with analogue signals and power supplies
- Pads from the AMS library for the digital signals and power supplies



3.9 Pad List

Pad	Location		Name	Description	Part	Direction	Cell	Type
	x	y						
1	64.35	75.4	temp	Temperature sensor			DirectPad_140	Direct pad
2	164.35	75.4	gnda!	analogue ground		I/O	AGND3ALLP140	Power
3	264.35	75.4	gnda!	analogue ground		I/O	AGND3ALLP140	Power
4	364.35	75.4	gnda!	analogue ground		I/O	AGND3ALLP140	Power
5	464.35	75.4	gnda_probe	analogue ground		I/O	AGND3ALLP140	Power
6	564.35	75.4	gnda_probe	analogue ground			AGND3ALLP140	Power
7	664.35	75.4	vdda_probe	Analogue power			AVDD3ALLP140	Power
8	764.35	75.4	vdda_probe	Analogue power			AVDD3ALLP140	Power
9	864.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
10	964.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
11	1064.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
12	1164.35	75.4	v_disc_ref1	VdiscriRef1, . Test pad (1)		I/O	APRIOP140	
13	1264.35	75.4	v_disc_ref1_probe	VdiscriRef1, . Test pad (1)			ProbePadL140	
14	1364.35	75.4	v_disc_ref2	VdiscriRef2, Test pad (1)		I/O	APRIOP140	
15	1464.35	75.4	v_disc_ref2_probe	VdiscriRef1, . Test pad (1)			ProbePadL140	
16	1564.35	75.4	i_test	Current reference of DAC, test pad		O	APRIOP140	
17	1664.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
18	1764.35	75.4	v_disc_clp	VdiscriClp, Test pad (1)		I/O	APRIOP140	
19	1864.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
20	1964.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
21	2064.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
22	2164.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
23	2264.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
24	2364.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
25	2464.35	75.4	v_clp	Clamping voltage for pixels			DirectPad_140	Direct pad
26	2564.35	75.4	v_clp	Clamping voltage for pixels			DirectPad_140	Direct pad
27	2664.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
28	2764.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
29	2864.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
30	2964.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
31	3064.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
32	3164.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
33	3264.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
34	3389.35	75.4	gnd_latch!	latch ground			AGND3ALLP140	Power
35	3489.35	75.4	gnd_latch!	latch ground			AGND3ALLP140	Power
36	3589.35	75.4	vdd_latch!	Digital power			AVDD3ALLP140	Power
37	3689.35	75.4	vdd_latch!	Digital power			AVDD3ALLP140	Power
38	3814.35	75.4	vdd!	Digital power			VDD3ALLP140	Power
39	3913.85	75.4	vdd!	Digital power			VDD3ALLP140	Power
40	4013.85	75.4	gnd!	ground			GND3ALLP140	Power

Pad	x	y	Name	Description	Part	I/O	Cell	Type
41	4114.35	75.4	gnd!	ground			GND3ALLP140	Power
42	4239.35	75.4	vddra_reg!	output voltage of VDDA regulator	Regulator		DirectPad_140	Power
43	4339.35	75.4	vddra_reg!	output voltage of VDDA regulator			DirectPad_140	Power
44	4439.35	75.4	vddra_reg!	output voltage of VDDA regulator	(optional)		DirectPad_140	Power
45	4539.35	75.4	vddra_reg!	output voltage of VDDA regulator			DirectPad_140	Power
46	4664.35	75.4	en_bandgap	enable band gap			ICDP140	
47	4764.35	75.4	dis_vdda1	disable the regulator			ICUP140	
48	4864.35	75.4	vddregin!	input digital power			VDD3ALLP140	Power
49	4964.35	75.4	vddregin!	input digital power			VDD3ALLP140	Power
50	5064.35	75.4	vddregin!	input digital power			VDD3ALLP140	Power
51	5164.35	75.4	vddregin!	input digital power	Regulator		VDD3ALLP140	Power
52	5264.35	75.4	gnd!	digital ground			GND3ALLP140	Power
53	5364.35	75.4	VBG	bandgap voltage, test pad	(optional)		DirectPad_140	
54	5464.35	75.4	VB_REG	voltage of reference current, test pad			DirectPad_140	
55	5589.35	75.4	gnd!	ground			GND3ALLP140	Power
56	5689.35	75.4	ext_pwrpulse	external power pulse enable			ICDP140	
57	5789.35	75.4	vdd!	digital power			VDD3ALLP140	Power
58	5889.35	75.4	vdd!				VDD3ALLP140	Power
59	5989.35	75.4	ext_disc_line	external line discriminator			ICDP140	
60	6089.35	75.4	gnd!	digital ground			GND3ALLP140	Power
61	6189.35	75.4	gnd!	ground			GND3ALLP140	Power
62	6289.35	75.4	speak_p_probe		Main Inputs		ProbePadL140	
63	6389.35	75.4	speak_p	Active readout marker and clock for analog.		I	PAD_LVDS_Rcv140	
64	6489.35	75.4	speak_n			I	PAD_LVDS_Rcv140	
65	6589.35	75.4	speak_n_probe				ProbePadL140	
66	6689.35	75.4	vdd!	digital power			VDD3ALLP140	Power
67	6789.35	75.4	vdd!	digital power			VDD3ALLP140	Power
68	6889.35	75.4	gnd_probe!	ground			GND3ALLP140	Power
69	6989.35	75.4	gnd!	ground			GND3ALLP140	Power
70	7089.35	75.4	start_p_probe				ProbePadL140	
71	7189.35	75.4	start_p	Synchronize the outputs		I	PAD_LVDS_Rcv140	DI-pulldown
72	7289.35	75.4	start_n			I	PAD_LVDS_Rcv140	DI-pulldown
73	7389.35	75.4	start_n_probe				ProbePadL140	
74	7489.35	75.4	vdd!	digital power			VDD3ALLP140	Power
75	7589.35	75.4	vdd_probe!	digital power			VDD3ALLP140	Power
76	7689.35	75.4	gnd!	ground			GND3ALLP140	Power
77	7789.35	75.4	gnd!	ground			GND3ALLP140	Power
78	7889.35	75.4	clkl_p_probe				ProbePadL140	
79	7989.35	75.4	clkl_p	Master clock, LVDS compatible		I	PAD_LVDS_Rcv140	LVDS-RX

Pad	x	y	Name	Description			Cell	Type
80	8089.35	75.4	clkl_n	Master clock, LVDS compatible		I	PAD_LVDS_Rcv140	LVDS-RX
81	8189.35	75.4	clkl_n_probe				ProbePadL140	
82	8289.35	75.4	vdd!	digital power			VDD3ALLP140	Power
83	8389.35	75.4	vdd!	digital power			VDD3ALLP140	Power
84	8489.35	75.4	gnd!	ground			GND3ALLP140	Power
85	8589.35	75.4	gnd!	ground			GND3ALLP140	Power
86	8689.35	75.4	clkd_n_probe		digital		ProbePadL140	
87	8789.35	75.4	clkd_n	Readout clock for digital data		O	LVDS-TX	DO LVDS
88	8889.35	75.4	clkd_p			O	LVDS-TX	DO LVDS
89	8989.35	75.4	clkd_p_probe		main		ProbePadL140	
90	9089.35	75.4	vdd!	digital power			VDD3ALLP140	Power
					output			
91	9189.35	75.4	do0_n_probe				ProbePadL140	
92	9289.35	75.4	do0_n	Data output, channel 0		O	LVDS-TX	DO LVDS
93	9389.35	75.4	do0_p			O	LVDS-TX	DO LVDS
94	9489.35	75.4	do0_p_probe				ProbePadL140	
95	9589.35	75.4	ground	ground			GND3ALLP140	Power
96	9689.35	75.4	do1_n_probe				ProbePadL140	
97	9789.35	75.4	do1_n	Data output, channel 1		O	LVDS-TX	DO LVDS
98	9889.35	75.4	do1_p			O	LVDS-TX	DO LVDS
99	9989.35	75.4	do1_p_probe				ProbePadL140	
100	10089.35	75.4	vdd!	digital power			VDD3ALLP140	Power
101	10189.35	75.4	mkd_n_probe				ProbePadL140	
102	10289.35	75.4	mkd_n	Marker for digital data		O	LVDS-TX	DO LVDS
103	10389.35	75.4	mkd_p			O	LVDS-TX	DO LVDS
104	10489.35	75.4	mkd_p_probe				ProbePadL140	
105	10589.35	75.4	gnd!	ground			GND3ALLP140	Power
106	10689.35	75.4	gnd!	ground			GND3ALLP140	Power
107	10789.35	75.4	vdd!	digital power			VDD3ALLP140	Power
108	10889.35	75.4	vdd!	digital power			VDD3ALLP140	Power
109	11014.35	75.4	gnd!	ground Memory			GND3ALLP140	Power
110	11114.35	75.4	gnd!	ground Memory			GND3ALLP140	Power

Pad	x	y	Name	Description			Cell	Type
111	11214.35	75.4	gnd!	ground Memory			GND3ALLP140	Power
112	11314.35	75.4	vdd!	digital power Memory			VDD3ALLP140	Power
113	11414.35	75.4	vdd!	digital power Memory			VDD3ALLP140	Power
114	11514.35	75.4	vdd!	digital power Memory			VDD3ALLP140	Power
115	11639.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
116	11739.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
117	11839.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
118	11939.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
119	12039.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
120	12139.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
121	12264.35	75.4	gnd!	ground			GND3ALLP140	Power
122	12364.35	75.4	clka	Readout clock for analogue data		O	BT4P140	3-state, 4 mA
123	12464.35	75.4	clka_probe				ProbePadL140	
124	12564.35	75.4	vdd!	digital power			VDD3ALLP140	Power
125	12664.35	75.4	mka	Analog marker		O	BT4P140	
126	12764.35	75.4	mka_probe				ProbePadL140	
127	12864.35	75.4	gnd!	ground			GND3ALLP140	Power
128	12964.35	75.4	vdd!	digital power			VDD3ALLP140	Power
129	13064.35	75.4	vdd!	digital power			VDD3ALLP140	Power
130	13164.35	75.4	vdd!	digital power			VDD3ALLP140	Power
131	13264.35	75.4	vdd!	digital power			VDD3ALLP140	Power
132	13364.35	75.4	gnd!	ground			GND3ALLP140	Power
133	13464.35	75.4	gnd!	ground			GND3ALLP140	Power
134	13564.35	75.4	tdo	JTAG data output		O	BT4P140	3-state, 4 mA
135	13664.35	75.4	tdo_probe				ProbePadL140	
136	13764.35	75.4	tdi	JTAG data input		I	ICUP 140	pullup
137	13864.35	75.4	tdi_probe				ProbePadL140	
138	13964.35	75.4	tms	JTAG mode state		I	ICUP 140	pullup
139	14064.35	75.4	tms_probe				ProbePadL140	
140	14164.35	75.4	tck	JTAG clock		I	ICCK2P140	clockin

Pad	x	y	Name	Description			Cell	Type
141	14264.35	75.4	tck_probe				ProbePadL140	
142	14364.35	75.4	vdd!	digital power			VDD3ALLP140	Power
143	14464.35	75.4	vdd_probe!	digital power			VDD3ALLP140	Power
144	14564.35	75.4	rstb	Asynchronous reset, active low		I	ISUP140	pullup, schmitt
145	14664.35	75.4	rstb_probe				ProbePadL140	
146	14764.35	75.4	gnd!	ground			GND3ALLP140	Power
147	14864.35	75.4	gnd!	ground			GND3ALLP140	Power
148	14964.35	75.4	gnd!	ground			GND3ALLP140	Power
149	15064.35	75.4	gnd!	ground			GND3ALLP140	Power
150	15164.35	75.4	vdd!	digital power			VDD3ALLP140	Power
151	15264.35	75.4	vdd!	digital power			VDD3ALLP140	Power
152	15364.35	75.4	clkc	clock CMOS		I	ICCK2P140	
153	15464.35	75.4	clkc_probe				ProbePadL140	
154	15589.35	75.4	vdd_latch!	digital power			AVDD3ALLP140	Power
155	15689.35	75.4	vdd_latch!	digital power			AVDD3ALLP140	Power
156	15789.35	75.4	gnd_latch!	ground			AGND3ALLP140	Power
157	15889.35	75.4	gnd_latch!	ground			AGND3ALLP140	Power
158	16014.35	75.4	gnd!	ground Memory			GND3ALLP140	Power
159	16114.35	75.4	gnd!	ground Memory			GND3ALLP140	Power
160	16214.35	75.4	gnd!	ground Memory			GND3ALLP140	Power
161	16314.35	75.4	vdd!	digital power Memory			VDD3ALLP140	Power
162	16414.35	75.4	vdd!	digital power Memory			VDD3ALLP140	Power
163	16514.35	75.4	vdd!	digital power Memory				Power
164	16639.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
165	16739.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
166	16839.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
167	16939.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
168	17039.35	75.4	gnda!	analogue ground			AGND3ALLP140	Power
169	17139.35	75.4	v_clp	Clamping voltage for pixels			DIRECTPAD_140	Direct pad
170	17239.35	75.4	v_clp	Clamping voltage for pixels			DIRECTPAD_140	Direct pad

Pad	x	y	Name	Description	Part	I/O	Cell	Type
171	17339.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
172	17439.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
173	17539.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
174	17639.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
175	17739.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
176	17839.35	75.4	vdda!	Analogue power			AVDD3ALLP140	Power
177	17964.35	75.4	vdda_reg	Ouput voltage of VDDA regulator	Regulator (optional)		DirectPad140	
178	18064.35	75.4	vdda_reg				DirectPad140	
179	18164.35	75.4	vdda_reg				DirectPad140	
180	18264.35	75.4	vdda_reg				DirectPad140	
181	18389.35	75.4	dis_vdda2	disable the regulator			ICUP 140	
182	18489.35	75.4	gnd!	ground			GND3ALLP140	Power
183	18589.35	75.4	vddregin!	input digital power			VDD3ALLP140	
184	18689.35	75.4	vddregin!	input digital power			VDD3ALLP140	
185	18789.35	75.4	vddregin!	input digital power			VDD3ALLP140	
186	18889.35	75.4	vddregin!	input digital power			VDD3ALLP140	
187	19014.35	75.4	vdd!	PLL digital power	PLL	I	VDD3ALLP140	Power
188	19114.35	75.4	dis_vcopll	disable pll vco		I	ICDP 140	
189	19214.35	75.4	seloutpll_tst	select pll output		I	ISUP 140	
190	19314.35	75.4	gnd!	PLL digital ground			GND3ALLP140	Power
191	19439.35	75.4	LVDS_gnd	LVDS ground supply			AGND3ALLP140	Power
192	19539.35	75.4	clk_pll_n	pll clock		O	pad_lvds_transmitter140	g_pad140
193	19639.35	75.4	clk_pll_p	pll clock		O		g_pad140
194	19739.35	75.4	LVDS_vdd	LVDS power supply			AVDD3ALLP140	Power
195	19864.35	75.4	gnd	PLL analogue ground			AGND3ALLP140	Power
196	19964.35	75.4	i_test_pll	pll test voltage, test pad			APRIOP140	
197	20064.35	75.4	vctl_pll	pll voltage control, test pad			APRIOP140	
198	20164.35	75.4	vdda	PLL Analogue power			AVDD3ALLP140	Power

Pad	x	y	Name	Description	Part	I/O	Cell	Type
200a	10138.75	22657	gnd_probe				g_pad140	
200b	9993.75	22657	gnd!	analogue ground			g_pad140	
201a	9828.75	22657	vdda_test_probe				g_pad140	
201b	9683.75	22657	vdda_test	analogue test power	For		g_pad140	
202a	9518.75	22657	anadriver_out0_probe				g_pad140	
202b	9373.75	22657	anadriver_out0	analogue driver test out 0		O	g_pad140	
203a	9208.75	22657	anadriver_out1_probe				g_pad140	
203b	9063.75	22657	anadriver_out1	analogue driver test out 1	analogue	O	g_pad140	
204a	8898.75	22657	anadriver_out2_probe				g_pad140	
204b	8753.75	22657	anadriver_out2	analogue driver test out 2		O	g_pad140	
205a	8588.75	22657	anadriver_out3_probe				g_pad140	
205b	8443.75	22657	anadriver_out3	analogue driver test out 3	test	O	g_pad140	
206a	8278.75	22657	anadriver_out4_probe				g_pad140	
206b	8133.75	22657	anadriver_out4	analogue driver test out 4		O	g_pad140	
207a	7968.75	22657	anadriver_out5_probe				g_pad140	
207b	7823.75	22657	anadriver_out5	analogue driver test out 5		O	g_pad140	
208a	7658.75	22657	anadriver_out6_probe				g_pad140	
208b	7513.75	22657	anadriver_out6	analogue driver test out 6		O	g_pad140	
209a	7348.75	22657	anadriver_out7_probe				g_pad140	
209b	7203.75	22657	anadriver_out7	analogue driver test out 7		O	g_pad140	

4 Glossary, abbreviations and acronyms tables.

Abbreviation or acronym	Meaning	Description
ad	Address	
adc	Analog to digital converter	
ana_	analog	
buf	buffer	
ce	Chip enable	
clk	clock	
clp	clamp	
cs	Chip select	
ct_	counter	
ctrl	control	
cur	current	
d	Data	
dac	Digital to analog converter	
dig_	digital	
dis_	disable	disable the internal signal high level active
disc	discriminateur	
en_	enable	Notation for internal signal high level active
etu	Elementary Time Unit	$ETU = 1timeclock = \frac{1}{main\_chip\_frequency} = \frac{1}{80MHz} = 12.5ns$
fifo	First in first out	Memory First In first Out,
jtg	jtag	Cf. JTAG interface IEEE 1149
ld	load	
lvds	Low voltage differential signaling	
mk	marker	
mux	Multiplexer	Structure that catches only nine groups of pixels among 6 x 15 groups. The first 9 states are kept.
patt	pattern	Here pattern of image.
pix	pixel	
pwr	power	
pwrs	Power save	
rd	read	
ref	reference	
rst	reset	Reset high level active
rst_n	reset	Reset low level active
rx	reception	
SDS	Sparse data scan	Asynchronous way to access from a hit to another hit. The next one has the priority
sel_	selection	

seq	sequencer	
suze	Suppression of zeroes	
sync	synchronization	
tck	Test clock	Cf. JTAG interface IEEE 1149
tdi	Test Data Input	Cf. JTAG interface IEEE 1149
tdo	Test Data Output	Cf. JTAG interface IEEE 1149
tms	Test Management System	Cf. JTAG interface IEEE 1149
tst	test	
tx	transmission	
wr	write	

Word or locution	Description
Pixel	Sensor unit element (surface: 20.7 x 20.7 µm)
bank	set of 64 pixels
Line, row	Set of 15 successive jointed bank (960 pixels)
Frame	The frame is a set of 928 lines.
Line duration	In default mode, 200 ns i.e. 16 times the period of the main internal clock 80 MHz.(12.5 ns)
Frame duration	= duration line x the content of the cycle Max register.